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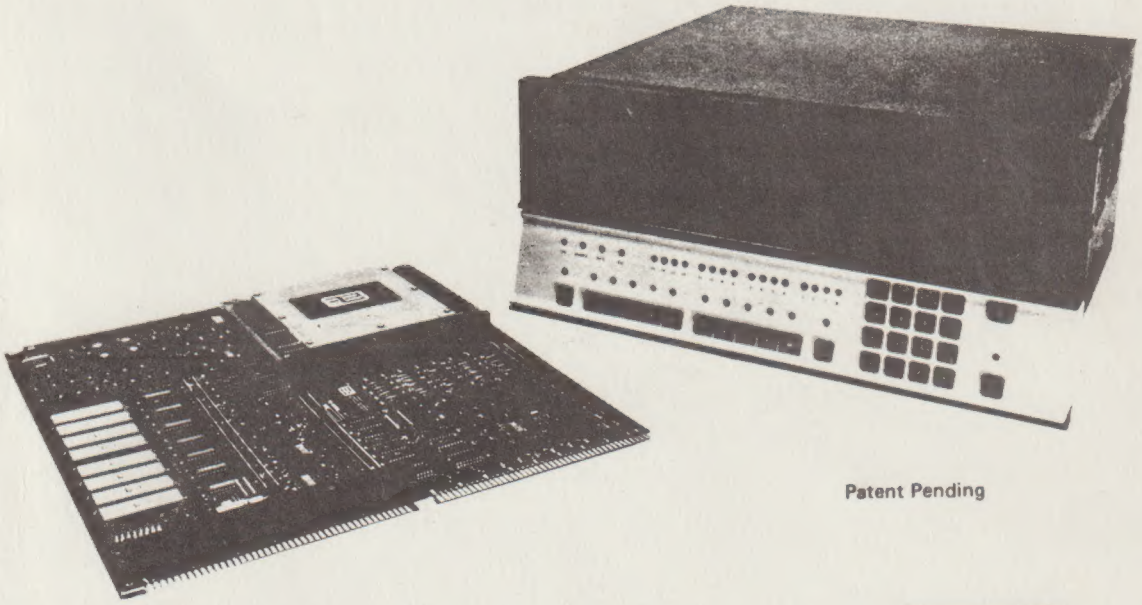
NAKED MINI®/ALPHA LSI SERIES

INTERFACE MANUAL



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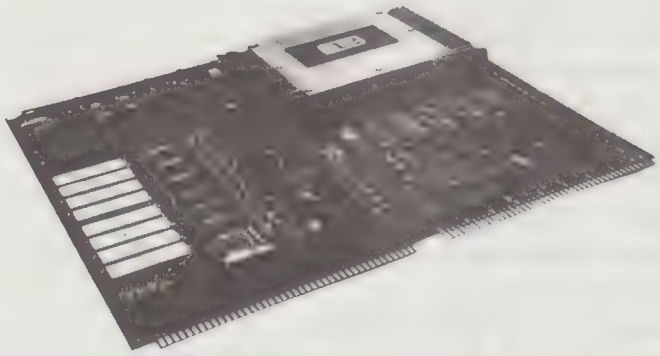

NAKED MINI LSI

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ALPHA LSI

Frontispiece. NAKED MINI LSI/ALPHA LSI Computers

Section 1
GENERAL INFORMATION

1.1 INTRODUCTION

The ALPHA LSI family of computers are highly flexible system components designed to be easily applied to control, communications, and monitoring tasks. These computers are extremely easy to program using assembly or machine language. Organization of the Processor enables the computer to obtain high memory efficiency, avoiding the problem of "core burning", so prevalent in many computers. Memory utilization is further enhanced by the powerful and flexible I/O command set. The I/O structure is simple and efficient, sharply reducing the amount of I/O logic required by units interfacing to the Processor.

To maximize the benefits of the Processor's unique I/O structure, careful consideration must be given to the design of the peripheral controller interfaces. This document presents comprehensive discussions of I/O (1) capability, (2) characteristics, (3) timing, (4) interrupts, (5) electrical design, (6) DMA controller design, (7) mechanical design, (8) integration, (9) console design, (10) power supply design, and (11) option card connections. The discussions that follow refer to the ALPHA LSI and NAKED MINI LSI Type 1 and Type 2 computers jointly as the ALPHA LSI computer.

1.2 CONTROL MODES

Two types of I/O instructions, select and sense, provide control information to and from an interface. The select instructions establish operating modes, control interrupts or initialize the interface. The sense instructions permit the Processor to obtain the operational status of an interface.

1.3 INPUT/OUTPUT MODES

The ALPHA LSI computer features five distinct I/O modes which when combined with an extensive set of I/O instructions provides a very powerful and easy to use I/O structure. These modes are:

1. Programmed I/O via registers
2. Programmed I/O via memory
3. Automatic I/O under interrupts
4. Block I/O
5. DMA

Transfers can be made to or from the A or X registers or directly to or from memory, whichever is more convenient. Both word and byte data can be handled directly, with byte data being packed automatically, if desired, without the need for time and space-consuming programmed routines.

1.3.1 Programmed Input/Output via Registers

For greater convenience in handling data that must be examined immediately upon input or is the result of computations that must be output immediately, programmed I/O transfers the data directly to and from the operating registers of the computer. Furthermore, programmed I/O instructions can be combined with sense and skip instructions to allow testing of controller or peripheral status prior to making a transfer.

1.3.2 Programmed Input/Output via Memory

This mode capitalizes on the power of the Automatic I/O instructions to transfer data to or from memory without disturbing the working registers of the computer. Any size block of data may be transferred into or out of memory at any address.

1.3.3 Automatic Input/Output under Interrupt Control

This mode permits an interface to transfer data to or from memory at its own data rate with minimal disturbance of the main program. When all data has been transferred, the interface develops an end-of-block interrupt in response to the Processor ECHO signal which, in turn, causes an interrupt subroutine to be entered which performs the necessary housekeeping associated with end-of-block operations.

1.3.4 Block Input/Otuput

For high speed transfer rates, Block I/O transfers block of any length. Data is exchanged directly between memory and the peripheral interface with the index register providing the word count. During Block I/O instructions, the computer is totally dedicated to the execution of the instruction and cannot respond to interrupts until the entire block has been transferred.

1.3.5 Direct Memory Access (DMA)

For very high speed transfer rates, the DMA handles data directly with the memory. Since this data transfer does not require the Central Processor, it can be performing other operations while interleaving with DMA on a cycle stealing basis. Multiple DMA controllers may use the DMA feature simultaneously (interleaved cycles) up to the full memory transfer rate. When more than one memory module is installed, memories may be two way interleaved to provide data transfer at twice the individual memory data rates.

1.4 DATA TRANSFER RATES

The maximum data transfer rates that can be achieved with the ALPHA LSI computer family are listed in Table 1-1.

Table 1-1. ALPHA LSI Family Maximum Data Transfer Rates

I/O MODE	LSI-1	LSI-2			
	C1600 C1200 C980 SC1200	C1600	C1200	C980	SC1200
DMA (Non Interleaved)	same as LSI-2	625,000 w/s	833,333 w/s	1,020,000 w/s	833,333 w/s
DMA (Interleaved)	same as LSI-2	1,250,000 w/s	1,409,000 w/s	1,666,666 w/s	1,666,666 w/s
Block In	131,579 w/s	444,444 w/s	454,545 w/s	458,711 w/s	454,545 w/s
Block Out	131,579 w/s	400,000 w/s	408,163 w/s	411,522 w/s	392,156 w/s
Programmed In (Cond) Word	34,247 w/s	112,369 w/s	130,718 w/s	136,040 w/s	124,223 w/s
Byte	34,247 b/s	112,369 b/s	125,896 b/s	130,718 b/s	119,760 b/s
Programmed Out (Cond) Word	34,247 w/s	112,994 w/s	131,578 w/s	135,135 w/s	126,582 w/s
Byte	34,247 b/s	112,994 b/s	126,582 b/s	129,870 b/s	122,222 b/s
Programmed In (Memory)	24,631 w/b/s	71,942 w/b/s	85,106 w/b/s	92,678 w/b/s	82,987 w/b/s
Programmed Out (Memory)	24,631 w/b/s	72,727 w/b/s	82,440 w/b/s	90,570 w/b/s	80,645 w/b/s
DMC In	26,738 w/b/s	63,091 w/b/s	74,627 w/b/s	82,101 w/b/s	73,529 w/b/s
DMC Out	26,738 w/b/s	62,111 w/b/s	73,260 w/b/s	81,766 w/b/s	71,684 w/b/s

w/s = words per seconds
b/s = bytes per seconds
w/b/s = words or bytes per seconds

Section 2

MAXI-BUS CHARACTERISTICS

2.1 INTRODUCTION

This section describes the signals and the electrical characteristics of the NAKED MINI LSI Computer Maxi-Bus. Additionally, the distribution of the Maxi-Bus and the ALPHA LSI Computer motherboard are discussed.

2.2 MAXI-BUS COMPONENTS (Figure 2-1)

The NAKED MINI LSI Computer Maxi-Bus consists of three major components: the Address bus (A), The Data bus (D), and the Control bus (C).

2.2.1 Address Bus (A)

The Address bus consists of 16 lines (AB00-through AB15-) that are time shared by the Processor and DMA controllers.

The Processor and DMA controllers use the 15 bits of the A bus to address memory locations. The 16th A bus bit (MSB) is used to specify word or byte memory operation. During I/O operations, the Processor uses the low order 8-bits of the A bus to convey device address and function code information to I/O devices. The high order 8-bits contain random information and are not normally used. The format of the low order 8-bits during I/O operations is as follows:

AB07-	Device Address bit 4	
AB06-	Device Address bit 3	
AB05-	Device Address bit 2	P Field
AB04-	Device Address bit 1	
AD03-	Device Address bit 0	
AD02-	Function Code bit 2	
AB01-	Function Code bit 1	F Field
AB00-	Function Code bit 0	

NOTE

The eight lines devoted to the Device Address and Function Code are arbitrarily divided into groups of five and three, respectively. They can be divided differently to increase or decrease the number of device addresses and function codes. For example, six lines can be devoted to the Device Address and only two to the Function Code. This would increase the number of device addresses to 64 and reduce the number of function codes to 4.

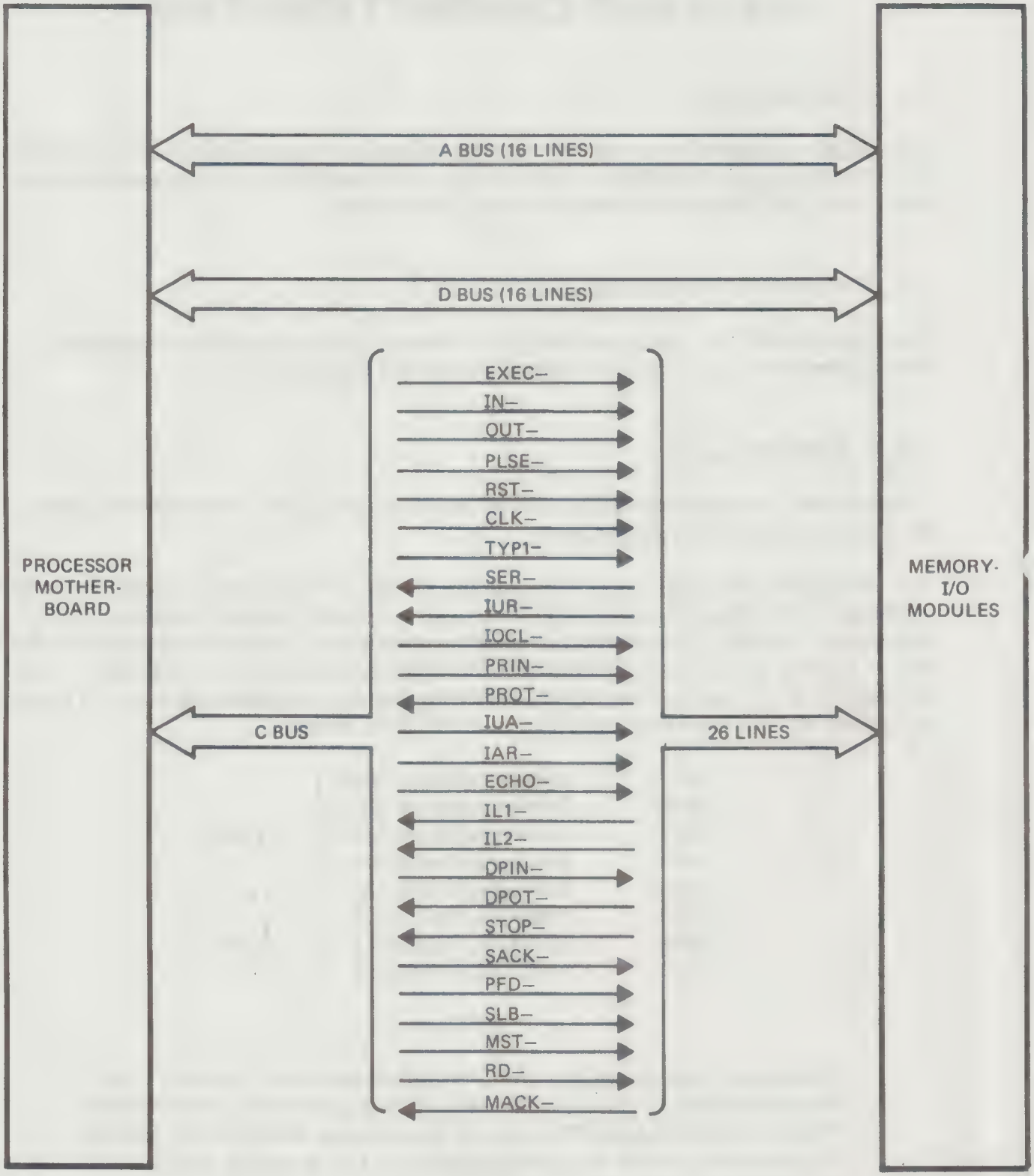


Figure 2-1. I/O Bus Components

Throughout the remainder of this design guide, all examples which involve I/O addresses assume the arbitrary five and three division.

2.2.2 Data Bus (D)

The Data bus consists of 16 bidirectional lines (DB00- through DB15-) that are time shared by the Processor, memory, and I/O interface controllers.

The Processor uses the D bus to read data from or write data into memory. Likewise, the Processor uses the D bus to transfer data to or from an I/O interface controller.

A DMA controller uses the D bus to read data from or write data into memory.

I/O interfaces use the D bus to convey an interrupt address to the Processor during interrupt processing.

2.2.3 Control Bus (C)

The C bus consists of 25 unidirectional control lines which define the specific action that an interface device is to perform. Seventeen lines are outputs from the Processor to all memories and interface controllers while eight lines are inputs from either memories or interface controllers to the Processor. The 25 C bus lines are subdivided into four broad categories: I/O command, utility signals, interrupt signals, and DMA signals. Except as noted below, all Processor generated or received signals may also be generated or received by DMA controllers during DMA operations.

2.2.3.1 I/O Commands

There are three signals in this category: EXEC-, IN- and OUT-. These signals define the type of I/O operation in process.

EXEC- Execute is a Processor generated signal that indicates that the current instruction is a Select or Select and Present instruction. EXEC- is used typically to set or reset controls in the addressed interface.

IN- Input is a Processor generated signal that indicates that the current instruction is an input instruction and that the addressed interface should place input data on the data bus.

OUT- Output is a Processor generated signal that indicates that the current instruction is an output instruction and that the Processor has placed output data on the data bus for the addressed interface controller to accept.

2.2.3.2 Utility Signals

There are five signals in this category: PLSE-, RST-, CLK-, TYP1-, and SER-.

PLSE- Pulse is a Processor generated signal which is used as a strobe pulse to load registers during an output transfer, set or reset controls during a Select instruction, reset data transfer controls during an input transfer, and to reset Interrupt Stimulus Store controls upon recognition of an interrupt.

RST- System Reset is a Processor or console generated signal which is used to reset all controls in ALL interfaces to a known starting configuration. RST- is generated by the Processor in response to a power failure condition, an Autoload Initiation sequence, or when the Console RESET switch is depressed. Note - not driven by DMA controllers.

CLK- Clock is a Processor generated, 1 megahertz, free-running square wave signal that may be used as a timing reference by interface controllers--it is not synchronized to Processor operations. Note that only the Processor generates this signal. DMA controllers may not generate this signal.

TYP1- Type 1 Processor Installed. This signal is ground-true when the type 1 Processor is installed and open when the type 2 Processor is installed. This signal permits DMA controllers to determine which Processor is installed and perform hog mode transfers if necessary. The TYP1- signal is strong through the "200" side of the motherboard only (see paragraph 2.4).

SER- Sense Response is a signal generated by an addressed interface controller to convey status to the Processor.

2.2.3.3 Interrupt Signals

There are nine signals associated with interrupt generation and processing. These signals are: IUR-, IOCL-, PRIN-, PROT-, IUA-, IAR-, ECHO-, IL1-, and IL2.

IUR- Interrupt Request is a multiplexed interrupt request line which multiple interfaces generate to request interrupt service. All interfaces which use this line are forced to compete with each other for recognition by the Processor. If two or more interfaces request interrupt service at the same time, recognition is given to the highest priority interface via the priority string. (PRIN- and PROT-).

IOCL- I/O Clock is a Processor generated signal which is used by interfaces to synchronize IUR interrupt requests into the Processor. IOCL has a minimum duration of 150 nanoseconds; however, the duration varies with internal Processor operation. When an interrupt is recognized by the Processor, IOCL is inhibited to prevent the generation of additional IUR interrupt requests. IOCL remains inhibited until the Processor completes execution of the interrupt instruction. DMA controllers may not generate this signal.

PRIN- and PROT- Priority In and Priority Out. PRIN- and PROT- form an interrupt priority chain which is strung serially through all interface controllers and memories. PRIN- is the name given to the priority chain where it enters an interface. If low, it allows the interface to generate interrupts. Each interface generates a PROT- signal to indicate that neither it nor other upstream devices are generating an interrupt. The PROT- signal from each interface is the PRIN- signal for the next downstream interface.

IUA- Interrupt Acknowledge is a Processor generated signal which goes true upon recognition of any interrupt and remains true during execution of the interrupt instruction. DMA controllers may not generate this signal.

IAR- Interrupt Address Request is a Processor generated signal which is used to request an interrupt address from an interface in response to an interrupt request. DMA controllers may not generate this signal.

ECHO- Echo is generated by the Processor when an Auto I/O instruction has transferred all data or by an IMS instruction when the count overflows. ECHO- is typically used by the interface to request an interrupt. This interrupt vectors to a user-determined location in memory which normally contains a JST instruction to a subroutine which performs the necessary housekeeping associated with an end-of-block or elapsed count operation. DMA controllers may not generate this signal.

IL1- and IL2- Interrupt Lines 1 and 2 are interface generated high priority interrupt request lines which interrupt to locations :0002 and :0006, respectively. They are higher priority than the IUR line. IL1 has priority over IL2. IL1 and IL2 do not require interrupt vectoring by the interface as does IUR.

2.2.3.4 DMA Signals

Nine signals are associated with DMA control and processing. These signals are: DPIN-, DPOT-, STOP-, SACK-, PFD-, SLB-, MST-, RD- and MACK-.

DPIN- and DPOT- — DMA Priority In and DMA Priority Out. DPIN and DPOT form a DM priority chain which is strung serially through all DMA controllers and memories. DPIN- is the name given to the priority chain where it enters a DMA controller. If low, it allows the controller to access memory. Each controller generates a DPOT- signal to indicate that neither it nor other upstream controllers are communicating with memory. The DPOT- signal from each controller is the DPIN- signal for the next downstream controller. The DPIN- and DPOT- signals are strung through the "200" side of the motherboard only (see paragraph 2.4).

STOP- — Stop Processor is a DMA controller generated signal which stops the Processor upon completion of its current machine cycle to permit the DMA controller to gain control of the I/O bus. STOP- may be generated at any time and may remain active for any length of time.

SACK- — Stop Acknowledge is a negative-true Processor generated signal which informs DMA controllers that the Processor is no longer controlling the I/O bus and that the DMA controllers may take over the I/O bus. SACK- will remain true until STOP- is removed.

PFD- — Power Failure Detected is a power supply generated signal which when active forces any DMA operations to terminate in order to permit the Processor to shut down the system in an orderly manner

SLB- — Select Least Significant Byte is a Processor or DMA controller generated signal which is used for Byte Mode memory accesses. When SLB- is low, the least significant byte (bits 0 through 7) of the addressed memory word is accessed. When SLB- is high, the most significant byte (bits 8 through 15) of the addressed memory word is accessed. SLB- is used to disable memory during Autoload operations by forcing it low while AB15- is high (word mode).

MST- — Memory Start is a Processor or DMA controller generated signal which is used to initiate a memory cycle.

RD- — Read Mode is a Processor or DMA controller generated signal which when low indicates the current memory cycle is a read/restore cycle. When high RD- indicates that the current memory cycle is a clear/write cycle. The Memory Protect options will force RD- low during any attempt to write into a protected memory location.

MACK- — Memory Acknowledge is a memory generated signal that is used to inform the Processor or DMA controller that data is available durin a read operation or that data has been accepted during a write operation.

2.3 ELECTRICAL CHARACTERISTICS

The Maxi-Bus is best classified as a hybrid tri-state open-collector (wire-OR) bus, unterminated.

Most Processor drivers are tri-state power elements, capable of sinking 32 mA at 0.4 Vdc maximum and sourcing 2.0 mA at 2.4 Vdc minimum. In a few isolated cases, open-collector TTL drivers (32 mA sink at 0.4 Vdc) are used.

Processor receivers present one standard TTL load to the line (-1.6 mA at 0.8 Vdc, 40 μA at 2.4 Vdc). Depending on the nature of the particular signal, pullup resistors to +5 Vdc are used.

Open-collector drivers in I/O and memory modules are permitted on those bus lines for which pullup resistors are provided. Minimum required drive capability is -32 mA at 0.4 Vdc max. Tri-state drivers electrically equivalent to the Processor bus drivers are also allowed, as long as the logic design of the system guarantees that no two tri-state drivers connected to the same bus line are simultaneously enabled. Receivers on I/O and memory modules may be any standard 74 series TTL device. Only one such receiver per module is permitted. Maximum loading shall not exceed 1.8 mA per module.

Logic Levels

(Negative-true)

logic "1": +0.4 Vdc max.
logic "0": +2.4 Vdc min.

Table 2-1 summarizes the driver, receiver and pullup circuits.

2.4 MOTHERBOARD ORGANIZATION

Any slot (other than the slot dedicated to the NAKED MINI LSI Processor) can accept either an I/O or memory module.

Figure 2-2 provides a diagram of the system motherboard. The motherboard provides for six slots used as follows:

Slot	Purpose
A	NAKED MINI LSI Computer
B	Universal (Memory or I/O)
C	Universal (Memory or I/O)
D	Universal (Memory or I/O)
E	Universal (Memory or I/O)
F	Power Supply

Table 2-1. Maxi-Bus Load, Drive and Termination Summary

	SIGNAL	PIN	DEVICE TYPE(S) (REFER TO NOTE 1) CPU	MEMORY	I/O CONT	DMA CONT	CONSOLE	BUFFER	OPT. BD
	GND	1							
	GND	2							
	-12.	3							
	+12.	4							
	+12.	5							
	-12	6							
	12.	7							
	12.	8							
NOTE 2	DPIN	9							
NOTE 2	DPOT	10		J]	J]				
NOTE 3		11							
NOTE 3		12							
	+5.	13							
	-5.	14							
	MST	15	1,6	5			5	5	5
		16							
	MACK	17	5,6	1					
	RD	18	2,6	5				1	2
NOTE 3		19						5	
	SLB	20	2,6	5					
	PFD	21	5,6					5	2
	MDIS	22	3	5					
	AB08-	23	1	5				5	
	AB09	24	1	5				5	
	AB10-	25	1	5				5	
	AB11-	26	1	5				5	
	GND	27							5
	GND	28							
	AB12	29	1	5					
	AB13-	30	1	5				5	5
	AB14-	31	1	5				5	5
	AB15	32	1	5				5	5
NOTE 2	TYP1	33	OPEN or GRD					5	
NOTE 3		34							
	STOP-	35	5,6						
	SACK-	36	3					2	
NOTE 2	MBIN	37		5				5	
NOTE 2	MBOT	38	4	4	J]	J]			
	DB00	39	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
	DB01-	40	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
	DB02-	41	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
	DB03-	42	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
	+5.	43							

SIGNAL	PIN	DEVICE TYPE(S) (REFER TO NOTE 1) CPU	MEMORY	I/O CONT	DMA CONT	CONSOLE	BUFFER	OPT. BD
+5V	44							
DB04	45	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB05	46	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB06	47	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB07	48	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB08	49	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB09	50	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB10	51	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB11	52	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB12	53	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB13	54	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB14-	55	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB15-	56	1,5,6	1,5	2,5	1,5	2,5	1,5	1
EXEC-	57	1,6		5	5	5	1,5	1
IN-	58	1,6		5	5	5	5	5
GND	59						5	5
GND	60							
IOCL-	61	1,6		5	5	5	5	5
OUT-	62	1,6		5	5	5	5	5
CLK-	63	3		5	5	5	5	
SER	64	5,6		2	2		2	2
IUR-	65	5,6		2	2		2	2
IL1-	66	5,6		2	2		2	
IAR-	67	1,6		5	5	5	5	5
IL2-	68	5,6		2	2		2	
RST-	69	2,5,6		5	5	2,5	2	5
IUA	70	1,6		5	5		5	
PLSE-	71	1,6		5	5	5	5	5
ECHO-	72	1,6		5	5		5	5
+5V	73							
+5V	74							
AB03-	75	1	5	5	1,5	5	5	5
AB04-	76	1	5	5	1,5	5	5	5
AB05-	77	1	5	5	1,5	5	5	5
AB06-	78	1	5	5	1,5	5	5	5
AB07-	79	1	5	5	1,5	5	5	5
AB00-	80	1	5	5	1,5	5	5	5
AB01-	81	1	5	5	1,5	5	5	5
AB02-	82	1	5	5	1,5	5	5	5
PRIN	83			5	5			5
PROT-	84	4	J]	4	4		•	4
GND	85							
GND	86							

NOTES 1. DEVICE TYPES ARE AS FOLLOWS-
1) TRI-STATE DRIVER, 32ma (8835 or EQUIV.)
2) 32 MA OPEN-COLLECTOR DRIVER (7438 or EQUIV
3) 32 MA TTL DRIVER (7437 OR EQUIV.)
4) 16 MA TTL DRIVER (7400 OR EQUIV.)
5) TTL RECEIVER (7404 OR EQUIV.)
6) PULL-UP RESISTOR (1 KOHM)
J) JUMPER
•) STRAIGHT THRU SIGNAL (NO DEVICES IN SIGNAL PATH

2. DPIN-, DPOT-, MBIN-, MBOT-, AND TYP1- ARE STRUNG THROUGH THE 200 SERIES CONNECTORS ONLY. THESE PIN POSITIONS ARE UNASSIGNED ON THE 100 SERIES CONNECTORS AND ARE RESERVED FOR FUTURE EXPANSION

3. THESE PINS CARRY SPECIAL SIGNALS ON SLOT A100 AND ARE RESERVED FOR FUTURE EXPANSION ON THE REMAINING 100 AND 200 SERIES CONNECTORS.

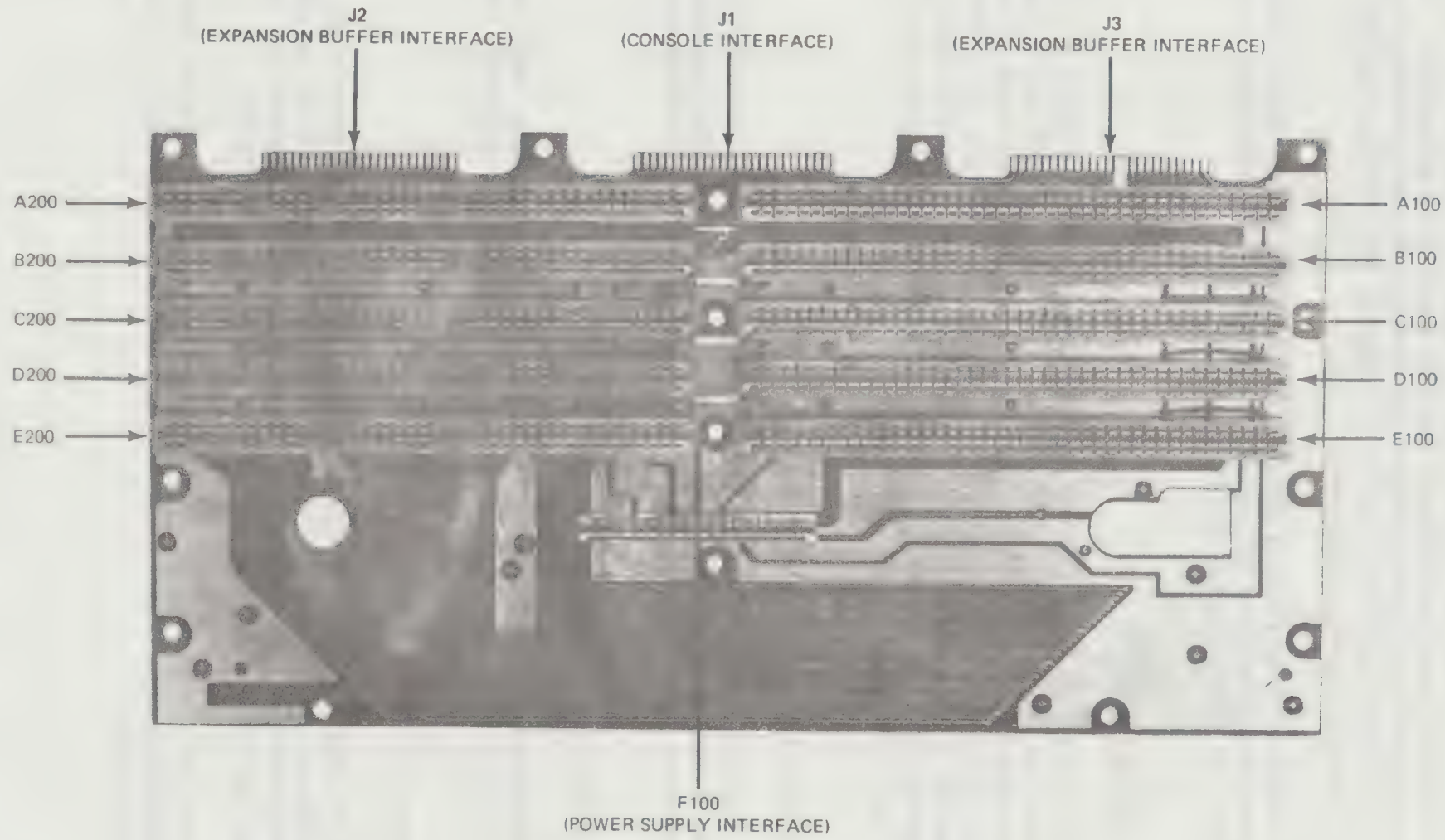


Figure 2-2. ALPHA LSI Motherboard Slot Organization (Rear View)

COMPUTER AUTOMATION, INC.

In any given slot, either a full-width card (15" x 16.5") or two half-width cards (each 7.5" x 16.5") may be installed. One slot contains two connectors. The pins on one connector of a slot are numbered 100 through 186, and is referred to as the 100-series connector; similarly, the other connector (pins 200 through 286) is referred to as the 200-series connector.

With the exception of the priority chains, memory bank control, and two special Processor power supply signals, all signals are wired in a U fashion through all half-card connectors. All exceptions are described below.

2.4.1 Interrupt Priority

The daisy-chained interrupt priority string (PRIN-, PROT-) is wired in S fashion beginning at the 100-series connector of slot A, across to the 200-series connector, then in reverse direction across the two B slot connectors, etc., until all slots are connected. Both ends of the chain are connected to the expansion connectors. Both PRIN- and PROT- on the Processor connector (100-series connector, slot A) are used to carry special signals to the console; the actual origin of the priority chain is therefore the Processor side of the top slot (slot A200).

2.4.2 Memory Bank Control, DMA Priority

The memory bank control (MBIN, MBOT), DMA priority (DPIN-, DPOT-) and TYP1- daisy-chains run down the 200-series connectors only. Therefore, memories and DMA controllers must be either full cards or half cards installed on the 200 series side only.

2.4.3 Processor Power Supply Signals

Two lines from the power supply, TTLF (twice the line frequency) and +5 H (hang power) wired directly between the power supply slot and Processor slot (slot A100).

2.5 EXPANSION

To facilitate expansion of the computer system beyond the first chassis and to provide for interconnect to the ALPHA LSI console, expansion connectors are supplied on the motherboard immediately above slot A. Two connectors are provided for Maxi-Bus expansion and one connector is provided to interconnect the console.

In the event that insufficient slots are provided in the basic ALPHA LSI chassis for a given application, the Maxi-Bus may be expanded via a buffer card, cables, and expansion chassis.

The expansion chassis is a second ALPHA LSI chassis (identical motherboard, etc.). A buffer card is required to regenerate the Maxi-Bus. Cables interconnect the buffer card to the two motherboards via the expansion connectors. The Maxi-Bus of the computer on the motherboard may not be extended without electrical buffering.

Expansion may extend to two, three or more chassis. As expansion chassis are installed, a speed degradation will occur. Memory modules located in expansion chassis will exhibit an apparent slower system access time. Similarly, I/O modules located in a second expansion chassis or beyond may require that the timing circuit of the Processor be altered to provide additional phase stretching during I/O operations (refer to Section 11). This timing circuit is modified simply by changing an option-jumper connector which configures all jumper-controlled Processor options in the machine. This option-jumper connector mounts to the rear-edge of the Processor option card.

2.6 NAKED MINI LSI MAXI-BUS REQUIREMENTS

In applications where the NAKED MINI LSI computer is used without the system motherboard and is instead connected to I/O and/or memory modules via user-supplied cabling, printed circuit card, etc., the line length of each signal must be limited to 18 inches.

The Maxi-Bus must be designed to minimize crosstalk, reflections, etc., so as to preserve signal integrity. Recommendations as to line termination are available upon request. In general, consultation with Computer Automation is recommended to ensure system performance.

2.7 TWO-MODULE OPTIONS

Any option requiring more than one printed circuit card may not use the motherboard for interconnection. Unique interconnections may be made via a jumper cable installed on the rear edge of the two cards.

Section 3
I/O TRANSFER TIMING

3.1 INTRODUCTION

This section describes the I/O transfer timing of the various I/O instructions. I/O transfer timing is the period during an I/O instruction when data is transferred between the Processor and an interface and is shown in Figure 3-1.

NOTE

Unless otherwise noted, all timing intervals indicated in timing diagrams are given in nanoseconds. All timing intervals discussed in text are nominal.

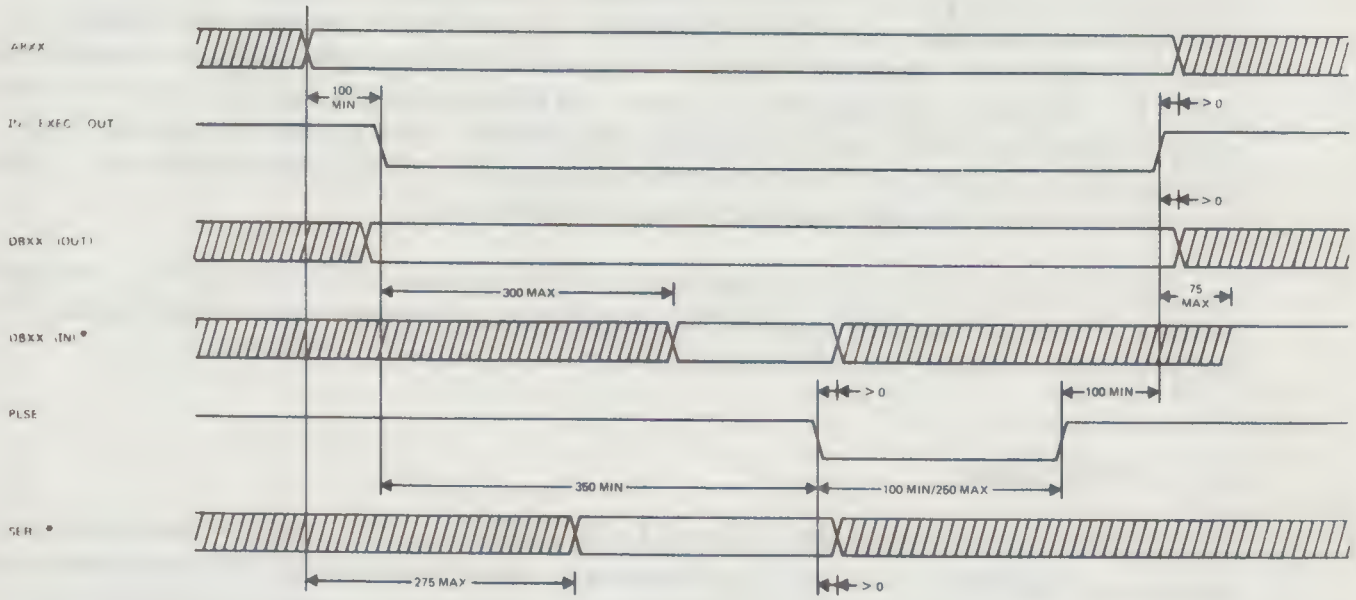


Figure 3-1. I/O Transfer Timing

3.2 I/O BUS CONSIDERATIONS

The A bus is active for non-I/O as well as I/O instructions. To guard against responding to a non-I/O instruction, the I/O control signals (EXEC-, IN- or OUT-) should be used when interpreting the A bus. The SER- signal is the only exception and may be driven independent of EXEC-, IN- or OUT-.

Data should never be placed on the D bus by an interface except in the presence of IN- or IAR-.

3.3 SENSE COMMAND TIMING

No Maxi-Bus control signals are generated by the Processor during a Sense instruction. The addressed interface controller uses the function code information to determine which one of eight possible functions are to be sensed. The sense information is sent to the Processor via the SER- line. If the Processor is looking for a sense response, the SER- signal is gated into the Processor, otherwise it is ignored. The user has 275 nanoseconds to stabilize the sense response after receipt of the Device Address signals.

3.4 SELECT COMMAND TIMING

During Select or Select and Present commands, the EXEC- signal is generated a minimum of 75 nanoseconds after the A bus stabilizes. The D bus is selected for output as a result of EXEC- and becomes stable a maximum of 150 nanoseconds after the leading edge of EXEC-. If a command register is used, the information on the D bus can be presented to the register by EXEC- and clocked in with PLSE-. The D bus contains all zeros during the SEL instruction and is equal to the contents of the Processor A or X register during the SEA or SEX instructions, respectively.

The PLSE- signal is developed a minimum of 350 nanoseconds after EXEC-. PLSE- is generally used to clock all control flip-flops in the interface. Either the leading or trailing edge of PLSE- may be used to set or reset control flip-flops.

3.5 INPUT TIMING

All input sequences, regardless of the Input command type, appear basically the same to an interface. For all Input commands, the IN- signal is generated a minimum of 75 nanoseconds after the A bus stabilizes. The D bus is selected for input as a result of IN-. The IN- signal is used by the interface to gate data onto the D bus. Data must be present and stable on the D bus no later than 300 nanoseconds after IN- goes low.

The PLSE- signal is developed a minimum of 350 nanoseconds after IN- goes low. PLSE- is typically used to reset the buffer ready control in the interface. Either the leading or trailing edge of PLSE- may be used to reset the buffer ready control. Note, however, that data on the D bus must remain stable until the leading edge of PLSE- and must be removed no later than 75 nanoseconds after the trailing edge of IN-.

If the Input command issued is conditional, the sense response (SER-) must be stable no later than 275 nanoseconds after the A bus stabilizes to guarantee detection of SER- by the Processor. If SER- is high from the 275 nanosecond point to the leading edge of PLSE-, the entire input sequence is repeated for a conditional input or block input until the SER- line goes low. If SER- is low at the 235 nanosecond point, the operation is terminated after the present cycle and PLSE- is generated to indicate that the Processor has accepted the data. If SER- changes state between the 275 nanosecond point and the leading edge of PLSE-, the Processor may or may not detect SER-.

All sense responses are ignored by the Processor when executing unconditional Input commands.

3.6 OUTPUT TIMING

All output instruction sequences, regardless of the output command type, appear basically the same to an interface. During an Output command, the OUT- signal is generated a minimum of 75 nanoseconds after the A bus stabilizes. The D bus is selected for output as a result of OUT-. Once selected, the D bus stabilizes in a maximum of 150 nanoseconds after the leading edge of OUT-.

The PLSE- signal is generated a minimum of 350 nanoseconds after OUT- goes low. PLSE- serves two functions. The first is to clock output data into a receiving register in the interface. The second function is to reset the output buffer empty control in the interface.

If the Output command is conditional, the sense response must be stable no later than 275 nanoseconds after the A bus stabilizes to guarantee detection of SER- by the Processor. If SER- is high from the 275 nanosecond point to the leading edge of PLSE-, the entire output sequence is repeated until the SER- line goes low. If SER- is low at the 275 nanosecond point, the operation is terminated after the present cycle and PLSE- is generated to indicate the availability of data to the interface. If SER- changes state between the 275 nanosecond point and the leading edge of PLSE-, the Processor may or may not detect SER-.

Any sense responses that are generated during an unconditional Output command are ignored by the Processor.

3.7 AUTOMATIC INPUT AND OUTPUT TIMING

The Automatic Input and Output commands have essentially the same transfer timing as all other I/O commands. The only difference is that when used as interrupt instructions they develop an ECHO- signal to the interface when the last word or byte of data has been transferred. The ECHO- signal occurs a minimum of 350 nanoseconds after IN- or OUT-during the last transfer. ECHO- is typicall used by the interface to develop an end-of-block interrupt. These commands are unconditional commands that do not require a sense response.

3.8 I/O INSTRUCTION LIST

For the convenience of the user, Table 3-1 provides a list of the Processor I/O instructions. The instructions are grouped into four major categories (sense, select, input and output). The input and output categories are further divided into unconditional, automatic, conditional and block sub-categories. The conditional and block sub-categories require a sense response while the unconditional and automatic sub-categories do not.

Table 3-1. I/O Command List

FUNCTION	MNEMONIC	MACHINE CODE (HEX)
Sense	SEN	49XX
	SSN	48XX
Select	SEL	40XX
	SEA	44XX
	SEX	46XX
Unconditional Input	INA	58XX
	INX	5AXX
	IBA	78XX
	IBX	7AXX
	INAM	5CXX
	INXM	5EXX
	IBAM	7CXX
	IBXM	7EXX
Automatic Input	AIN	50XX
	AIB	54XX
Conditional Input	RDA	59XX
	RDX	5BXX
	RBA	79XX
	RBX	7BXX
	RDAM	5DXX
	RDXM	5FXX
	RBAM	7DXX
	RBXM	7FXX
Block Input	BIN	71XX
Unconditional Output	OTA	6CXX
	OTX	6EXX
	OTZ	68XX
Automatic Output	AOT	60XX
	AOB	64XX
Conditional Output	WRA	6DXX
	WRX	6FXX
	WRZ	69XX
Block Output	BOT	75XX

XX = device address and function code

Section 4
INTERRUPT CHARACTERISTICS

4.1 INTRODUCTION

Minicomputers perform in a wide variety of applications where they communicate with many different types of devices. These devices operate at widely varying speeds and generate events that occur randomly rather than at evenly spaced time intervals. If the events do occur at evenly spaced time intervals, these intervals may be relatively far apart. For these reasons, a versatile and efficient computer needs a priority interrupt system.

If a computer does not have a priority interrupt system, the computer must poll all of the external devices which may require service. The polling must be at frequent enough intervals so that events are serviced within a reasonable time after they occur. Polling consumes considerable time, and may not allow much processing time between the handling of external events.

A priority interrupt system relieves the computer of the polling responsibility. The computer may continue processing data between external events, and may take time out from main program processing to handle external events as they occur.

The NAKED MINI/ALPHA computers feature four levels of interrupts. Each interrupt level uses an interrupt-request line to get the attention of the Processor. Upon getting the attention of the Processor, the source of the interrupt vectors the Processor to an interrupt location in memory. The interrupt location contains an interrupt instruction which defines the specific action that the Processor is to take in processing the interrupt.

The interrupt request lines are designated: Power Fail Interrupt (PFI); Console/TRAP Interrupt (CINT); Interrupt Line 1 (IL1); Interrupt Line 2(IL2); and Interrupt Request (IUR). A priority level exists between each of these lines wherein PFI has the highest priority, CINT is second, IL2 is third, IL2 is fourth and IUR is lowest in priority. PFI, CINT, IL1 and IL2 are self-vectoring lines (the user does not have to supply the interrupt address). The IUR line is shared by multiple devices and features a priority chain to resolve priority when two or more devices issue an IUR interrupt request at the same time. Each of the multiple interrupt sources that share the IUR line cause the Processor to be vectored to distinct locations that can be anywhere in memory.

4.2 INTERRUPT LINES

The characteristics of each of the four interrupt request lines are discussed in the following paragraphs.

4.2.1 Power Fail Interrupt

The Power Fail Interrupt (PFI) services the power down interrupt only. PFI is the highest priority interrupt line in the interrupt system and is not accessible to the user via the Processor Maxi-Bus.

4.2.2 Console (TRAP) Interrupt

The Console (TRAP) Interrupt (CINT) services the console interrupt and trap interrupt only. CINT is the second highest priority interrupt line and is not accessible to the user via the Processor Maxi-Bus.

4.2.3 Interrupt Line 1

Inerrupt Line 1 (IL1) vectors all interrupts to memory location : 0002. The memory parity option uses IL1, however, the parity error interrupt forces IL1 to vector to memory location : 0012. IL1 does not provide external priority resolution when servicing multiple devices. IL1 is the third highest priority interrupt line and is accessible to the user via the Processor Maxi-Bus.

4.2.4 Interrupt Line 2

Interrupt Line 2 (IL2) vectors all interrupts to memory location : 0006. IL2 is the fourth highest priority interrupt line and is accessible to the user via the Processor Maxi-Bus. Like IL1, IL2 does not provide external priority resolution to service multiple devices.

4.2.5 Interrupt Request

The Interrupt Request (IUR) vectors interrupts to the Processor from virtually an unlimited number of devices. The IUR line has a priority string associated with it. The priority string insures that a device with a higher priority will be serviced before a lower priority device when two or more IUR requests occur at the same time. When the interrupting device has priority, it must furnish an interrupt address to the Processor upon request. In general, IUR interrupt addresses are user defined.

4.3 PROCESSOR GENERATED INTERRUPTS

The LAPHA LSI computer generates two standard and six optional interrupts. In addition, two optional pseudo interrupts are generated. Each of these interrupts are discussed briefly in the following paragraphs in order of priority.

4.3.1 Power Fail/Restart Interrupt (Optional)

The Power Fail/Restart Option (PF/R) generates a power-down interrupt to location : 001C whenever a low power condition exists. The power-down interrupt has the highest priority of any interrupt processed by the Processor. When power is restored to an acceptable level, the PF/R logic causes the program counter to be set to location : 0000 and the RUN mode is established to restart the system. Although location : 0000 is the power-up location, it is not a true interrupt location but rather a pseudo interrupt since no interrupt processing is required to get to location : 0000.

4.3.2 Autoload (Optional)

The Autoload option utilizes the PF/R logic to develop a pseudo-interrupt to location : 0000 of a special Autoload read-only-memory as a starting point for the Autoload sequence.

4.3.3 Console Interrupt and Trap (Standard)

A console interrupt can be developed when the Processor is in the RUN mode and the INT switch on the console is depressed. A trap interrupt is developed when the TRP instruction is executed. Both the console and trap interrupt share the second-highest interrupt priority and they both interrupt to location : 001E.

4.3.4 Memory Parity (Optional)

The Memory Parity option generates a parity error interrupt to location : 0012 via the IL1 line whenever a parity error is detected during a memory read operation. The parity error interrupt is the highest priority interrupt on the IL1 line but is lower in priority than the power-down, console and trap interrupts.

4.3.5 Real Time Clock (Optional)

The Real-Time Clock (RTC) option generates a clock and sync interrupt. The clock and sync interrupts share the second highest priority on the IUR line. The clock interrupt is vectored to location : 0018 while the sync interrupt is vectored to location : 001A.

4.3.6 Teletype Interface (Optional)

The processor mounted TTY Interface generates both word and end-of-block interrupts via the IUR line. The word interrupt is vectored to location : 0002 while the end-of-block interrupt is vectored to location : 0006. These interrupt vectors are the same interrupt vectors that are used by the IL1 and IL2 lines. Since IL1 and IL2 do not provide priority resolution and are of a higher priority than these interrupts, the TTY word and end-of-block interrupts should be displaced to alternate locations when IL1 and IL2 are used. A jumper option permits the word and end-of-block interrupts to be displaced to locations : 0022 and : 0026, respectively. When used in the full duplex mode the teletype interface generates four interrupts (locations : 0002, : 0006, : 0022, and : 0026).

4.4 OFFSETTING PROCESSOR GENERATED INTERRUPTS

Figures 4-1 lists in the order of their absolute priority, the standard interrupt locations for all Processor generated interrupts. These interrupt locations are all located in the scratchpad area of memory. A jumper option permits the user to offset these locations by : 100 locations to place them outside the scratchpad area to allow more efficient utilization of the scratch area. IUR interrupts generated by non-processor mounted options may be individually offset to place them outside of the scratch area.

NOTE

The power-up restart and autoload start-up location (location : 0000) is not affected by the offset jumper option.

4.5 PERIPHERAL GENERATED INTERRUPTS

Peripheral interface controllers may request interrupt service via the IL1-, IL2- or IUR- request lines. The techniques used to develop these interrupt requests are discussed in detail in Section 5 of this design guide.

4.6 INTERRUPT TRANSFER TIMING (Figure 4-2)

For the purpose of priority resolution, all interrupts must be synchronized prior to being generated. Synchronization can occur only during a main-line program instruction. This is to insure that when executing the interrupt instruction, no other interrupt can intervene. When synchronization is obtained, the PROT- signal from the interrupting device goes high (false) to disable all down-stream IUR interrupts. When interrupts of higher priority than IUR are serviced, the Processor removes the PROT- signal (to the false state) to disable all IUR interrupts.

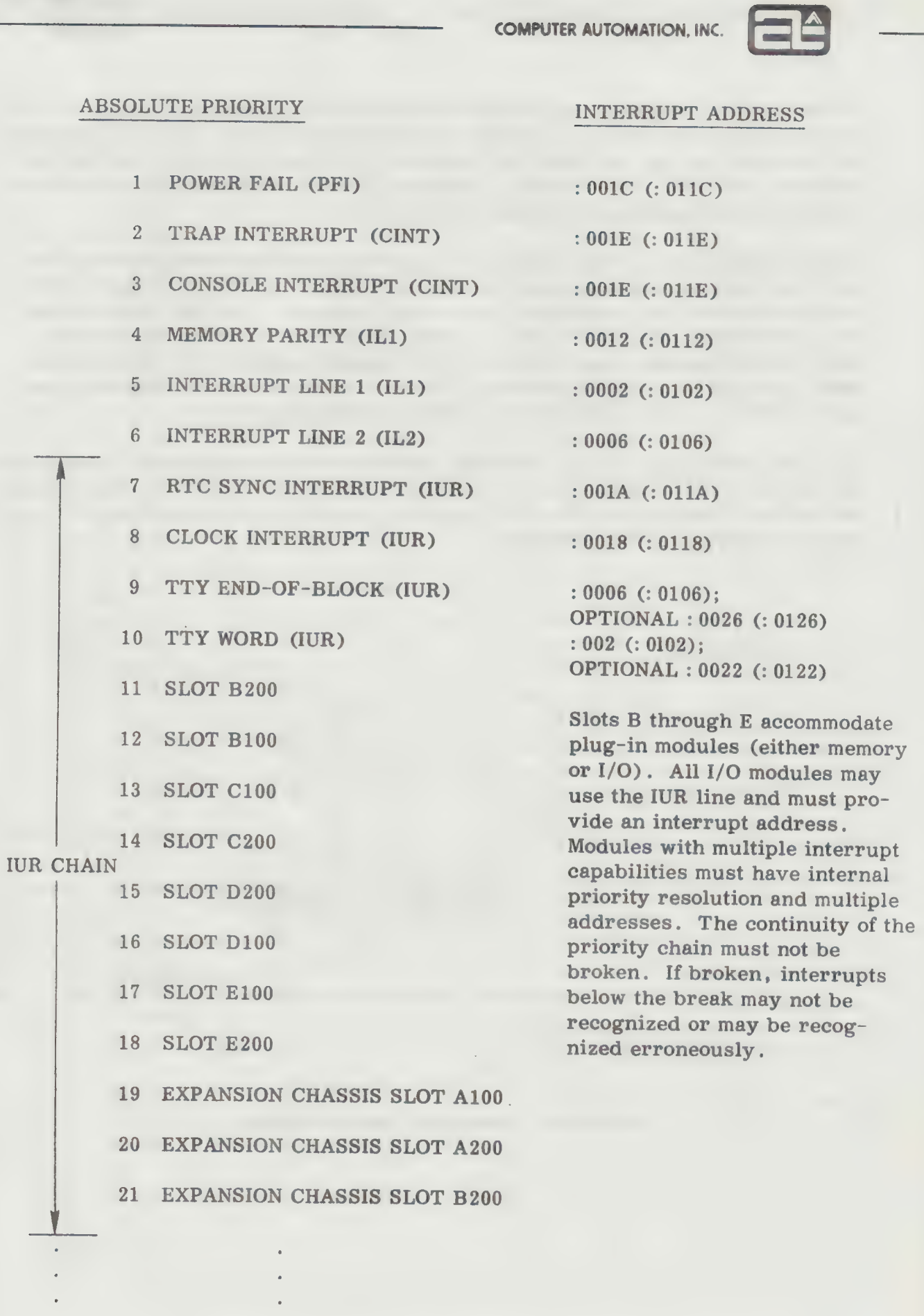

ABSOLUTE PRIORITY
INTERRUPT ADDRESS
1 POWER FAIL (PFI)
: 001C (: 011C)
2 TRAP INTERRUPT (CINT)
: 001E (: 011E)
3 CONSOLE INTERRUPT (CINT)
: 001E (: 011E)
4 MEMORY PARITY (IL1)
: 0012 (: 0112)
5 INTERRUPT LINE 1 (IL1)
: 0002 (: 0102)
6 INTERRUPT LINE 2 (IL2)
: 0006 (: 0106)
7 RTC SYNC INTERRUPT (IUR)
: 001A (: 011A)
8 CLOCK INTERRUPT (IUR)
: 0018 (: 0118)
9 TTY END-OF-BLOCK (IUR)
: 0006 (: 0106);
OPTIONAL : 0026 (: 0126)
10 TTY WORD (IUR)
: 002 (: 0102);
OPTIONAL : 0022 (: 0122)
11 SLOT B200
12 SLOT B100
13 SLOT C100
14 SLOT C200
IUR CHAIN
15 SLOT D200
16 SLOT D100
17 SLOT E100
18 SLOT E200
19 EXPANSION CHASSIS SLOT A100
20 EXPANSION CHASSIS SLOT A200
21 EXPANSION CHASSIS SLOT B200
Slots B through E accommodate plug-in modules (either memory or I/O). All I/O modules may use the IUR line and must provide an interrupt address. Modules with multiple interrupt capabilities must have internal priority resolution and multiple addresses. The continuity of the priority chain must not be broken. If broken, interrupts below the break may not be recognized or may be recognized erroneously.

Figure 4-1. ALPHA LSI Interrupt Organization

If interrupts are enabled, the Processor recognizes an interrupt request when the current main-line program instruction has finished execution. When recognition of an interrupt is given, the Interrupt Acknowledge signal (IUA) is issued by the Processor and IOCL is turned off to inhibit any change in interrupt request status until the current interrupt operation is completed.

Approximately 2 microseconds after IUA- goes low, the Processor generates the Interrupt Address Request signal (IAR-) and selects the D bus for input. IAR- is used by the interface to generate the interrupt address. The IAR- signal is low for approximately 750 nanoseconds. During this interval, the user generated interrupt address must be available within 300 nanoseconds of IAR- and remain stable until the leading edge of PSLE-. PLSE- is used in the more complex interrupt structures to reset the Interrupt Stimulus Store Control.

IUA- will remain low until the interrupt instruction finishes execution. The duration IUA- is low is a function of the number of machine cycles that are required to execute the interrupt instruction. When IUA- goes high, IOCL is re-enabled permitting subsequent interrupts to be generated.

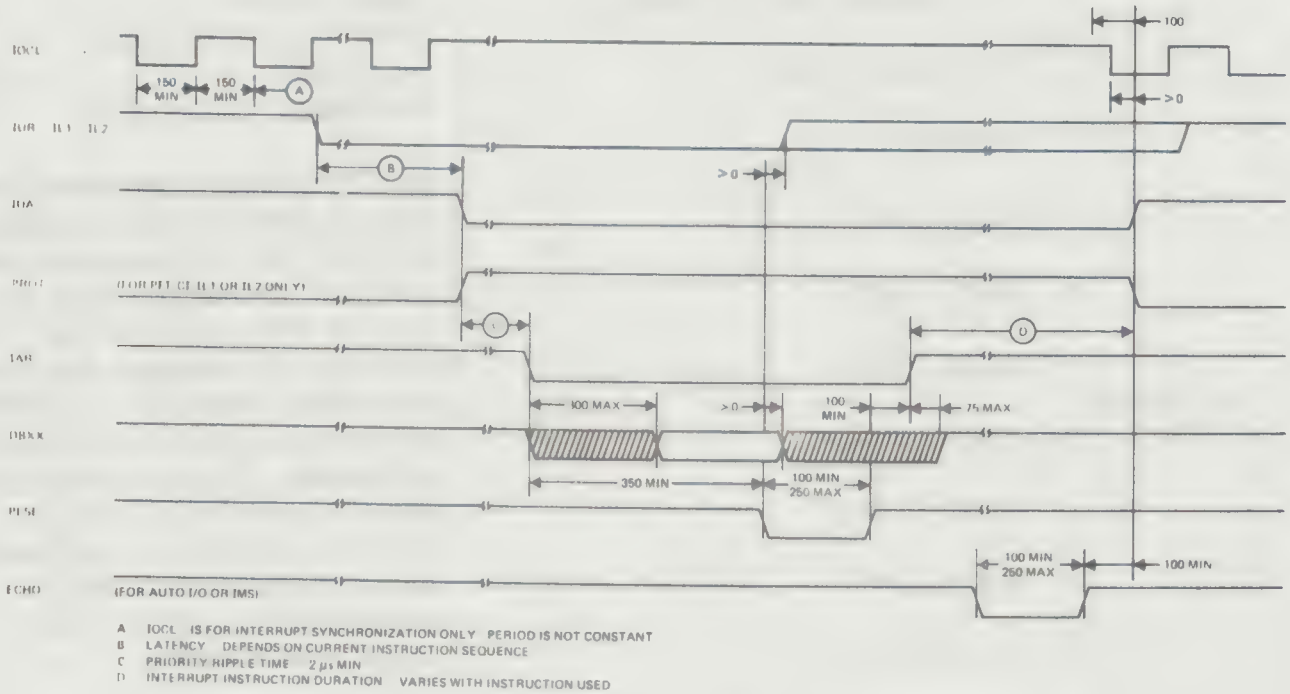


Figure 4-2. Interrupt Transfer Timing

4.7 INTERRUPT OPERATION CONTROL

Two levels of control are associated with IL1, IL2 and IUR interrupt processing--primary and secondary. The primary control level is provided by the Enable Interrupt flip-flop (EIN) in the Processor. The EIN flip-flop is accessible to the programmer and can be enabled or disabled on command. When enabled, EIN allows recognition of any interrupt. Likewise, when EIN is disabled, interrupts will not be recognized.

The secondary control level is provided by an interrupt enable flip-flop in each interface controller. The interrupt enable flip-flop enables or disables the interrupt structure of the interface controller. Like the EIN flip-flop discussed above, the interrupt enable flip-flop in each controller can be enabled or disabled by means of a select command addressed to the specific interface with the appropriate function code.

This dual system of interrupt control can be very useful to a programmer. With this system, the programmer can control interrupts in general with the EIN flip-flop, yet enable or disable interrupts from selected devices as conditions dictate.

Interrupts developed via the PFI and CINT lines are somewhat different in that they can be generated outside EIN control. In normal operation (that is, when operating under EIN control), the power fail, console and trap interrupts require that EIN be enabled. Most interrupt subroutines disable interrupts during execution of the subroutines causing high priority interrupts such as power fail to wait until EIN is re-enabled. A special jumper on the option board permits all interrupts generated on the PFI and CINT lines to be recognized regardless of the state of EIN.

When the jumper option is employed, two new instructions (PFE and PFD) are used to control the Power Fail circuits. The PFE instruction must have been issued before a Power fail interrupt can be generated. Likewise, the PFD instruction disables the generation of a power fail interrupt.

The Console Interrupt is controlled by the CIE and CID instructions in the same way as in normal operation. The trap interrupt is generated in the same manner as in normal operation. The only difference between normal operation and the jumper option is that EIN does not have to be set to generate the console and trap interrupts.

Another useful programming feature is the SIN instruction. The SIN instruction permits the programmer to suppress recognition of all interrupts (and Byte mode operation) for up to six instructions.

Once an interrupt structure is enabled, an interrupt can be generated in five basic steps:

Step 1 Stimulus Generation--The user generates the interrupt stimulus in response to some event or condition.

Step 2 Interrupt Request Generation--The interrupt structure of the interface controller, if enabled, stores the interrupt stimulus and generates an interrupt request.

Step 3 Interrupt Recognition--The Processor upon receipt of the interrupt request waits for the current instruction to finish execution, and if system interrupts are enabled (EIN set), issues an interrupt address request.

Step 4 Interrupt Address Generation--The interrupt structure of the interface controller responds to the interrupt address request by placing the interrupt address on the I/O data bus lines (except for IL1 and IL2 interrupt).

Step 5 Interrupt Instruction Execution--The Processor fetches and executes the instruction from the interrupt location.

4.8 INTERRUPT REQUEST LINE TRADE-OFFS

The user has a choice of three interrupt request lines, IL1, IL2 and IUR. The trade-offs associated with each of these lines are discussed below.

The IL1 and IL2 interrupt structures are the simplest structures to implement in terms of hardware since they do not require interrupt address logic, Processor synchronization logic, or down-stream priority disable logic. All of these functions are provided in the Processor. The IL1 and IL2 lines are intended for single device applications where high speed devices require the highest available priority

The IUR line is for multiple devices where each device competes for service via the priority chain. The priority of an interface controller can be changed by simply removing the interface controller from the computer chassis and relocating it in a higher or lower priority card slot. An IUR generating interface has greater flexibility in terms of address vectoring. If an address vector must be changed, the address may be offset from its base location to another location by means of address select lines.

Section 5

DEVICE INTERFACE CONTROLLER, DESIGN TECHNIQUES

5.1 INTRODUCTION

This section describes how to design a device interface controller that will be compatible with the I/O structure of the ALPHA LSI computer. The logic circuits described here are from Computer Automation, Inc. standard interface products that are successfully performing at user installations throughout the world.

5.2 I/O CONTROL IMPLEMENTATION

The following paragraphs describe device interface controller design requirements for compatibility with the I/O structure of the Processor.

5.2.1 Device Address Decoder (Figure 5-1)

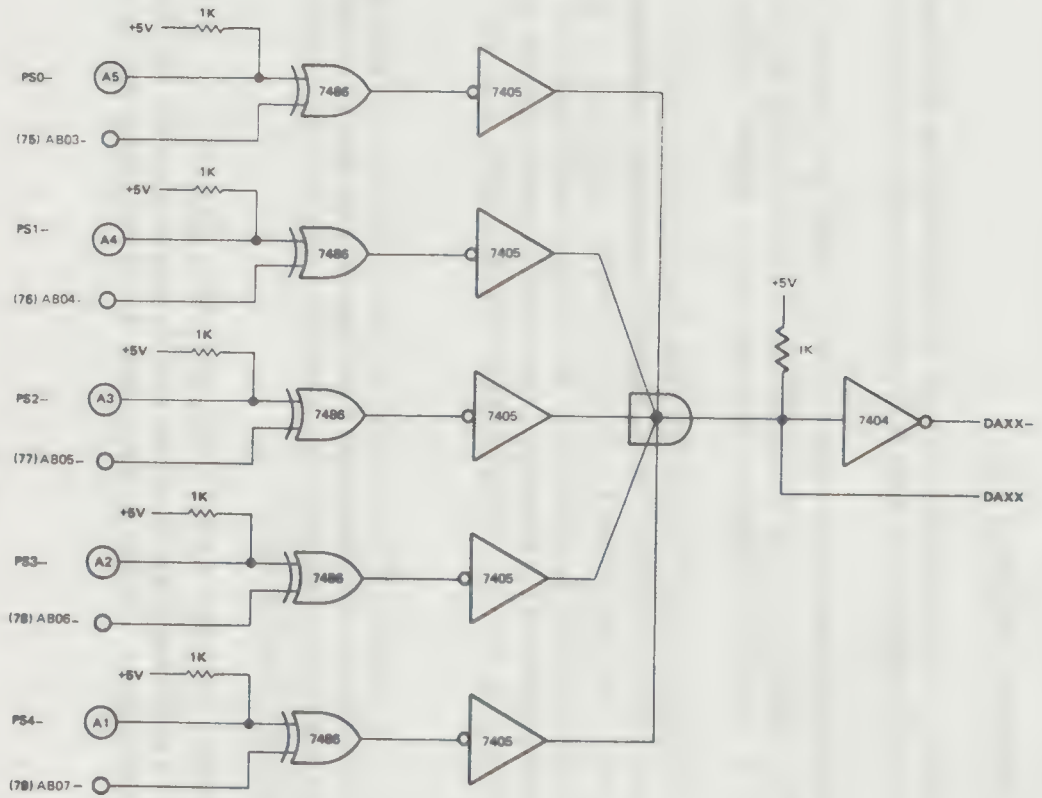
The device address decoder is a comparator circuit which compares the five-bit device address field of an I/O instruction with the user assigned device address.

The example A address decoder uses an exclusive-OR (EX OR) gate and an inverter for each of the five device address bits to be decoded. The outputs of the inverters are tied together to form a wired-AND address decoder output signal, DAXX.

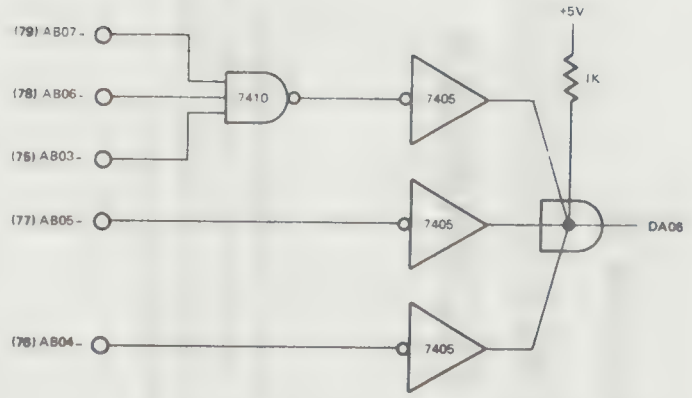
Address decoding is controlled by the five Peripheral Select signals (PS0- through PS4-). These signals are brought in from the peripheral interface connector to corresponding EX OR gates. If a true (low) address bit is to be decoded, the corresponding address select signal must be externally wired to ground (ground = true). Likewise, if a false address bit is to be decoded, the address select signal must be left open permitting the pull-up resistor to provide the false (high) address select signal.

When the device address bit agrees with the address select signal, the output of the EX OR gate is low. All five device address bits must agree with the user defined address selection. If agreement is obtained, the decoder output signal DAXX goes high enabling recognition of I/O commands.

Example B shows an address decoder which decodes device address : 6. This type of decoder is used only in dedicated applications and does not provide the flexibility that the example A decoder offers. Refer to Appendix A for standard device address assignments.



Example A. Non-Dedicated Application



Example B. Dedicated Application

Figure 5-1. Device Address Decoding Techniques

CAUTION

Device address : 00 should not be used. This address is reserved for Processor, options, the console as well as certain control instructions. Using it will cause improper operation of the Processor. Furthermore, a device interface connector containing properly installed device address jumpers must be applied to the rear-edge connector at all times. If it is not, a default address of : 00 will be assigned to the module, causing the same problem referred to above.

5.2.2 Function Decoder (Figure 5-2)

The Function Decoder uses an MSI chip, or a network comprised of SSI chips to decode the contents of the Function Bus. The result is a function code (1 of 8 maximum) which performs some function in the selected device interface controller.

The choice of chips depends upon the user's application. Figure 5-2 shows three examples, A, B and C of how to implement the function decoder. When decoding three or less functions, example C may be the most efficient. However, if chip count is a factor, example A or B is probably more efficient. In any case, where more than three functions are to be decoded, example A or B is probably the most efficient.

5.2.2.1 Example A

Example A uses a TTL 7442 MSI chip which is a 4 to 10 Decoder. Inputs A, B and C are the 2^1, 2^2, and 2^3 inputs respectively. Input D is the 2^4 input. When high, input D enables decoded output 8 or 9. However, only the first eight outputs of the decoder (0 through 7) are normally used, since eight is the maximum capacity of the three Function Bus lines in its normal configuration. D input is the enable input for the first eight decoded outputs, and utilizes the DAXX- signal for this purpose. When the device address is decoded, the DAXX- signal goes low, thus enabling the Function Decoder.

Input lines from the Function Bus are first unloaded by inverter gates and then applied to the decoder. As an example, if all Function Bus lines were false (high, implying Function Code 0), lows would be applied to inputs A, B and C. The decode of all low inputs would be zero thus causing FC0- to go low. (Decoded outputs of a 7442 are always low.) If a high signal is required, it can be obtained by using a simple inverter gate, such as the TTL 7404 illustrated.

5.2.2.2 Example B

Example B is the same as example A, except that the outputs are reversed (output 7 = FC0, output 6 = FC1, etc.). However, example B can only be used where the

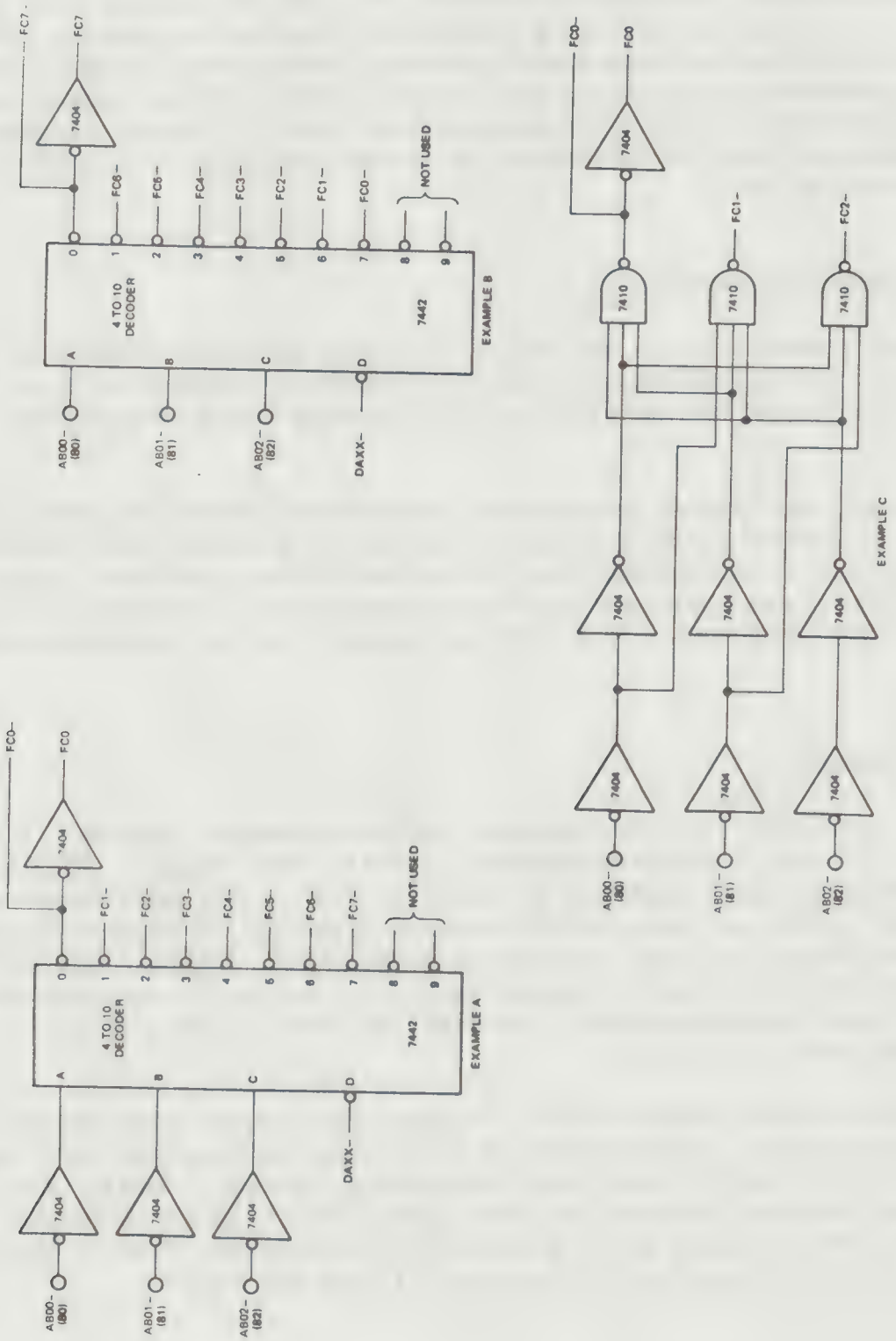


Figure 5-2. Function Decoder Configurations (Typical)

Function Bus lines will not be applied to any other circuit on the same device interface controller. This complies with the rule that each controller represents no more than one load to each I/O line.

5.2.2.3 Example C

Example C can decode only three function codes. TTL 7410 3-input NAND gates are the decoders. The three Function Bus signals are applied to the appropriate NAND gates to produce FC0- through FC2-. If the decoded device address is to enable the function codes, TTL 7420 NAND gates can be used, with the DAXX signal applied to the fourth input of each gate.

5.2.3 Select, Input or Output Command Decoding (Figure 5-3)

Similar to the Function Decoder, the Select, Input or Output (I/O) commands can be decoded by an MSI chip or a network of SSI chips. Figure 5-3 shows two methods, example A and B, of implementing this circuit. When the various commands are fully decoded using the F bus signals, the Function Bus decoder alone is not generally needed.

5.2.3.1 Example A

Example A shows a TTL 7442 4 to 10 Decoder used as a Select, Input or Output command decoder. The decoder also decodes the contents of the Function Bus, but only for the specific type of I/O command with which it is being used. Assume the decoder is used as a Select command decoder. The contents of the Function Bus are applied to the A, B and C inputs to produce the appropriate function code--any one of up to eight associated with the Select command. The decoder is enabled by NANDing DAXX (device address decoded), EXEC and PLSE. The Select command and associated functions are decoded by the one circuit. Refer to paragraph 2.4 for Select command timing.

5.2.3.2 Example B

Example B shows a decode network of SSI chips. This circuit can offer greater efficiency than the 7442 chip, depending upon the application. For example, if three types of commands (Select, Input and Output) are used by a controller, and less than three functions are associated with each type command, it is probably more efficient to use decoders of this type, each utilizing the outputs of a single Function Decoder.

5.2.4 Initialization Implementation (Figure 5-4)

Initialization circuitry establishes a known static state within a device interface controller. Initialization is started by executing a Select command with a function code

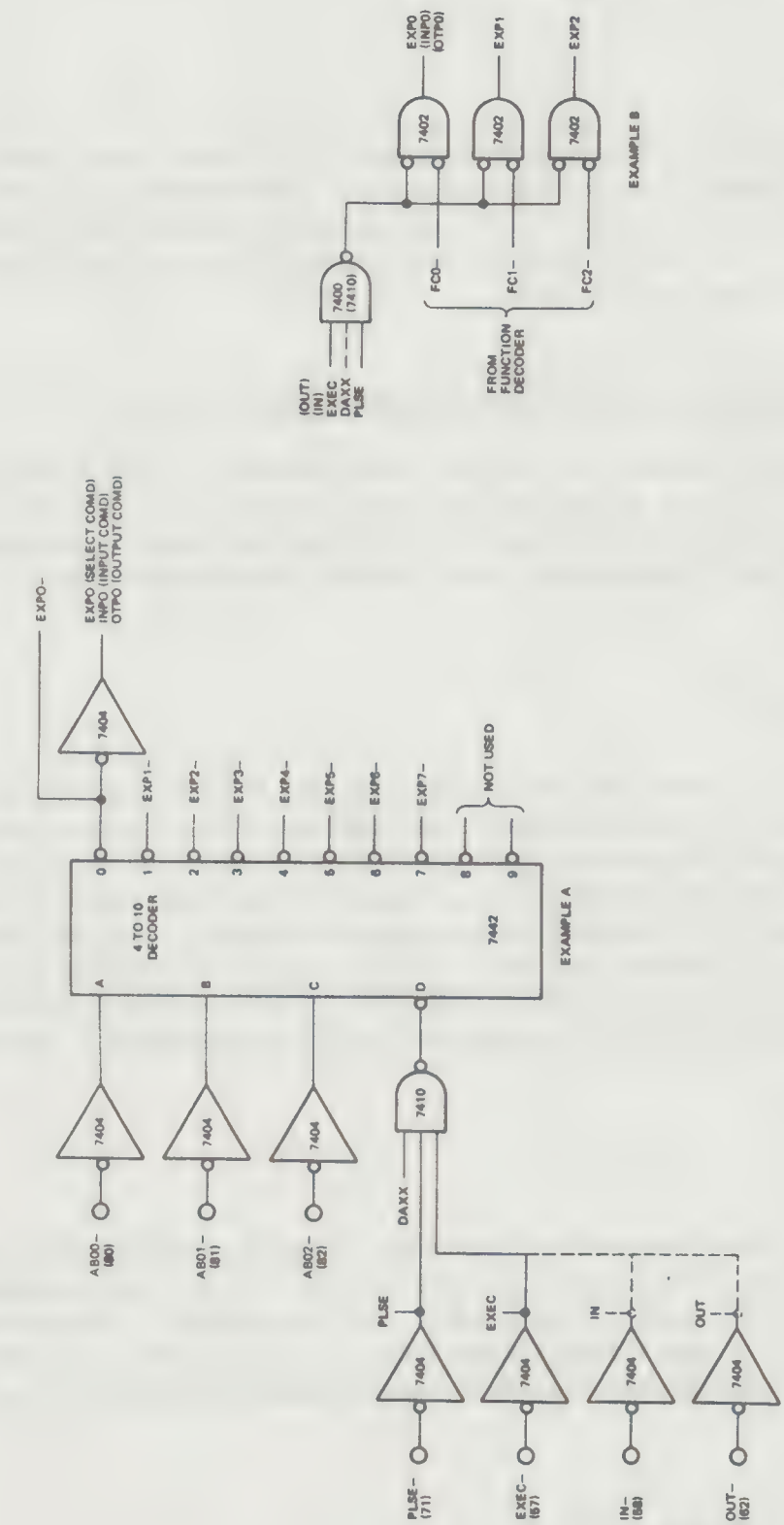


Figure 5-3. Select, Input or Output Command Decode Configurations

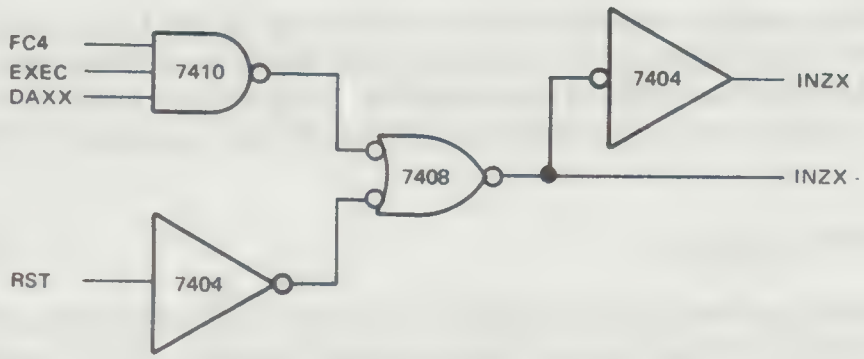


Figure 5-4. Initialization Circuit

dedicated to initialization (nominally Function Code 4) or by depressing the RESET switch on the Processor Control Panel. Figure 5-4 shows a circuit configuration for implementing initialization. When the device address and function code of the Select command are decoded, the DAXX and FC4 signals go high to prime the 3-input NAND gate. EXEC goes high during the Select command, enabling the gate to produce the INZX- and INZX signals. These signals are distributed throughout the controller to reset or set flip-flops, data registers, counters, etc., to establish the known static state. INZX is also produced when the RST- signal goes low upon depression of the RESET switch on the front panel, or during a power fail/restart situation.

5.2.5 Sense Command Implementation (Figure 5-5)

The Sense command circuit can be implemented using an MSI chip or a network comprised of SSI chips. As in the Function and I/O command decoders, application determines the most efficient method. An MSI chip can accommodate up to eight sense conditions, and provide its own function decoding. (Function code determines sense condition to be interrogated.)

The SSI network can be implemented more efficiently where three or less sense conditions are to be interrogated. However, the circuit requires inputs from a Function Decoder. Both positive and negative, internal and external signals can be sensed. An example of each is described below and illustrated in Figure 5-5.

5.2.5.1 Positive Sensing

Example A shows positive sensing using a TTL 74151 MSI chip. The 74151 is an 8 to 1 Multiplexer that provides internal function code decoding and an enable input (STROBE). It also provides both true and complement outputs. The top four inputs (0 through 3) are shown accepting External Sense (ES0 through ES3) signals from the external device. Pull-up resistors should be connected to each external input line (10K typical). Internal Sense (IS4 through IS7) signals are applied to inputs 4 through 7. When the device address is decoded, the multiplexer is enabled by DAXX- at the Strobe input. The outputs of the Function Bus unloading gates are applied to the decode input of the multiplexer (A, B and C). The appropriate sense signal, as determined by the function code, is then applied to the two outputs. Only the high output (Y) is used in this case. The signal is inverted and applied to the Sense Response line (SER-) by the 7438 driver. When the Y signal is high, the SER- line goes low. When the Y signal is low, the SER- line stays high.

Example B shows positive sensing using SSI chips. Both external and internal sensing is again illustrated. A separate Function Decoder is required to provide the necessary function codes. NAND gates combine the sense lines with the associated function codes. The outputs of the NAND gates are connected in a wire-ORed configuration to the SER- line.

5.2.5.2 Negative Sensing

Example C shows negative sensing using the 74151 MSI chip. Negative sensing is similar to positive sensing, except that the low output (W) of the chip is employed, rather than the high output, the strobe input is grounded to permanently enable the chip and DAXX is used to gate the multiplexer output onto the SER- line. As with positive sensing, all external sense lines should be provided with pull-up resistors.

Example D shows negative sensing using SSI chips. The negative-true signals are inverted and applied to 7438 2-input NAND gate drivers. Function code signals enable the appropriate driver. The outputs of the drivers may be connected in a wire-ORed configuration before being applied to the SER- line.

5.3 DATA TRANSFER CONTROL IMPLEMENTATION (Figure 5-6)

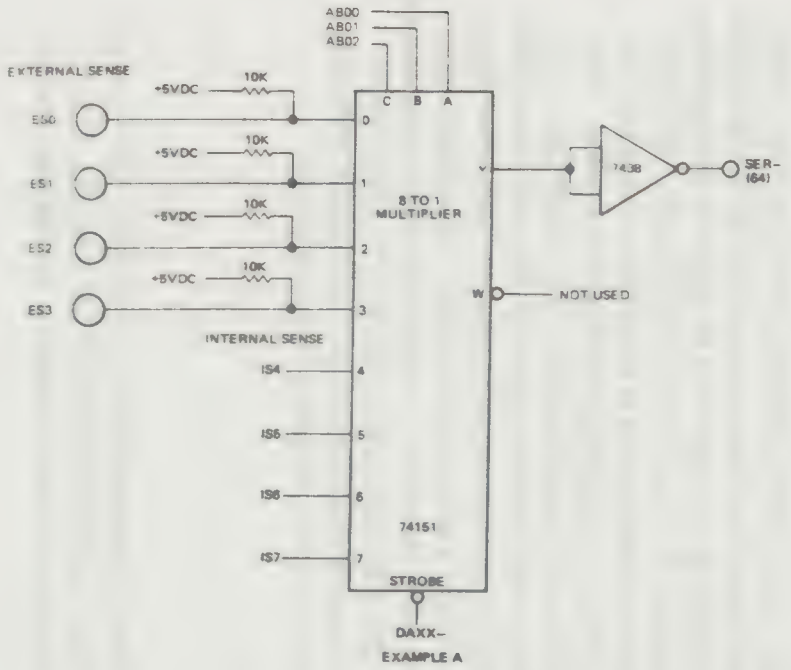
The efficient transfer of data between the Processor and device interface controller is controlled by the various buffer control circuits shown in Figure 5-6. An Output Buffer Empty circuit controls the transfer of data from the Processor to the interface (Examples A and B). An Input Buffer Full circuit controls the transfer of data from the interface to the Processor (Examples C and D).

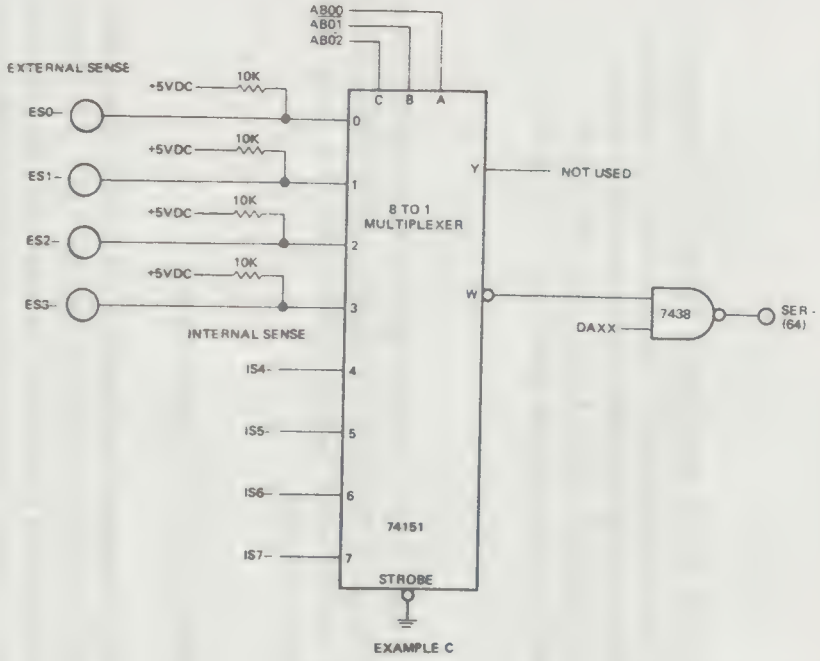
5.3.1 Example A

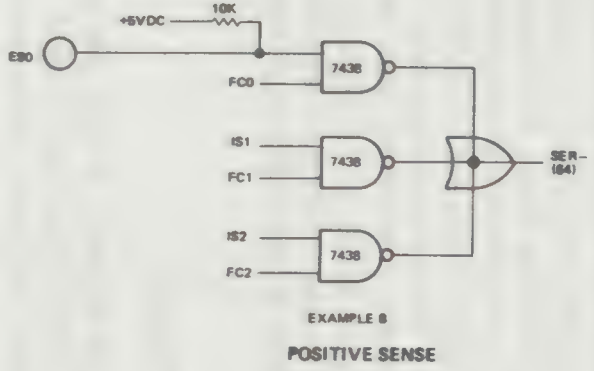
Example A shows an Output Buffer Empty latch (OBE) comprised of two TTL 7400 negative input NOR gates. The latch is initially set upon execution of the Initialize command for the controller. The INZX signal goes high and is applied through the NOR gate to the set side of the latch, causing it to set. The OBE signal thus goes high and is applied to the Sense Multiplexer from which it can be interrogated by Sense or Conditional Output commands using the appropriate function code. The OBE signal can also cause an interrupt through implementation of interrupt logic. When data is transferred to the controller Output Buffer, the DAXX, OUT and PLSE signals go high, enabling the NAND gate whose output is applied to the reset side of the latch. The latch now resets, inhibiting response to further interrogations by the Processor. When the data has been transmitted, a signal should be generated to indicate completion of the transfer. (Data Transmitted--DXMT). DXMT is applied to the same NOR gate as INZX, causing the latch to set again and indicate that the buffer is ready for more data at the next Processor interrogation.

5.3.2 Example B

The circuit in example B does the same thing as example A. The only difference is a TTL 7474 D type flip-flop is used, rather than the dual NOR gate latch. INZX- direct sets the flip-flop. The high OBE signal is then available for interrogation.







NOTE: FOR EXAMPLES B & D, ALL FUNCTION CODE DECODES MUST BE DEVELOPED USING DAXX AS IN FIG. 5-2 EXAMPLES A & B.

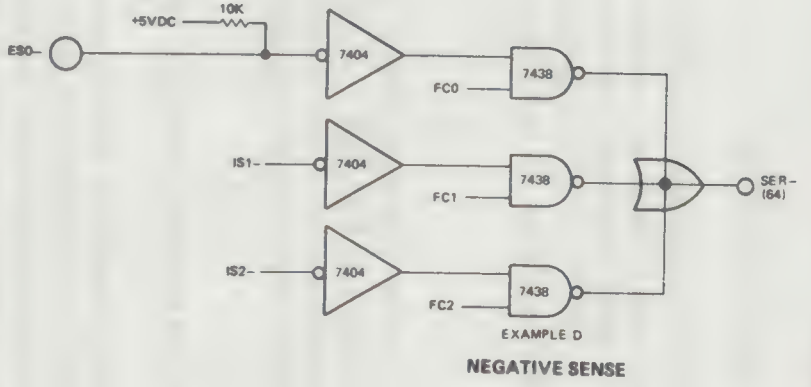


Figure 5-5. Positive and Negative Sense, Circuit Configurations

COMPUTER AUTOMATION, INC.

When data is transferred to the Output Buffer, the flip-flop is direct reset. When DXMT- goes true, the flip-flop is once again set to indicate the buffer is ready to accept more data.

5.3.3 Example C

Example C shows a latch configuration of an Input Buffer Full circuit (IBF). The latch is reset by INZX upon initialization of the controller. After data has been transferred to the Input Buffer, a signal should be generated to indicate the completion of the transfer (Data Received--DRCV). DRCV- sets the latch, causing IBF to go high. The IBF signal is then applied to the Sense Multiplexer where it can be interrogated by the Processor with Sense or Conditional Input commands. IBF can also cause an interrupt when implemented in the interrupt logic. When the data is transferred to the Processor, the DAXX, IN and PLSE signals go high, resetting the latch.

5.3.4 Example D

Example D shows an Input Buffer Full circuit using a TTL 7474 D type flip-flop. The flip-flop is direct reset upon initialization. The flip-flop is set when data is received (DRCV goes high). The flip-flop is then direct reset when the data is transferred to the Processor (DAXX, IN and PLSE go true).

5.4 PERIPHERAL DEVICE INTERRUPT IMPLEMENTATION

The design requirements for various interrupt structures compatible with the ALPHA LSI Computers are now discussed.

5.4.1 Interrupt Address Rationale

In general, interrupts are vectored to the first 256 words of memory. The main advantage for having interrupts vectored to this area of memory is in the housekeeping associated with certain interrupt instructions. An Auto I/O instruction, for instance, must have the word/byte count and address pointer redefined after a block of data has been moved. An IMS instruction must have the count value redefined after it has overflowed. If the interrupt instructions are in the first 256 words of memory, direct addressing can be used from anywhere in memory to update the instruction parameters in anticipation of the next interrupt pass.

In applications where the use of the first 256 words of memory for interrupts makes programming difficult, all interrupts can be offset :100 locations into the next 256 words of memory.

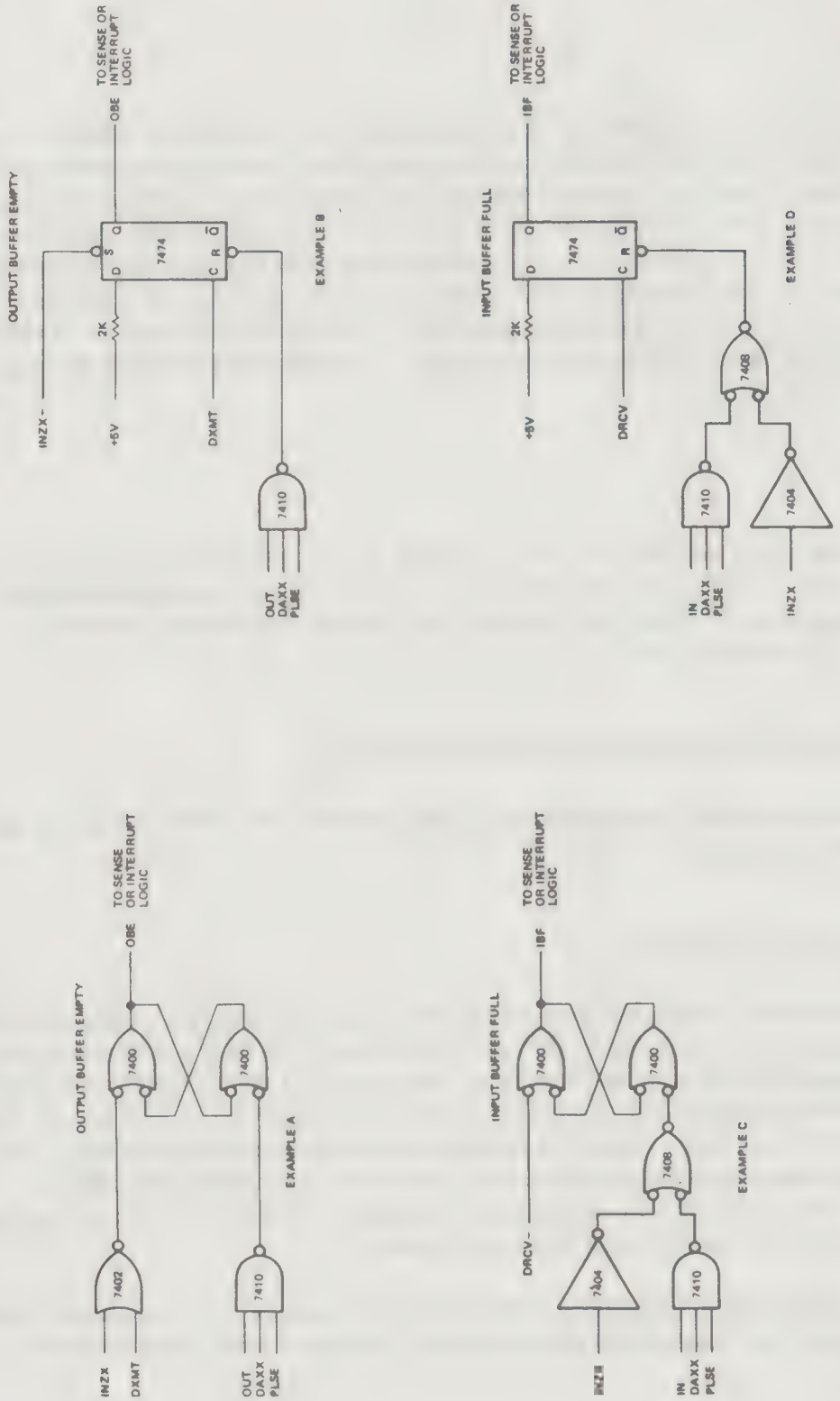


Figure 5-6. Data Transfer Control

The number of memory locations that are reserved for interrupts varies with each interface controller. If the interface controller is intended to move data under Auto I/O interrupt control, four locations should be reserved for the Auto I/O instruction and two locations for the Echo interrupt. If a simple tranfer of control is required, only two locations are required for a JST instruction. If external events are being counted, four locations must be reserved--two for the IMS instruction and two for the Echo interrupt.

If multiple interrupts are developed by an interface, these interrupts are organized into a family. Referring to Appendix A, the Real Time Clock option has a four word interrupt family and the 103 Data Set Controller has a 16-word family. Family size is strictly a function of the number of interrupts an interface develops and the number of locations required by each interrupt instruction.

To preserve compatibility throughout the ALPHA computer family, interface controllers are designed to interrupt to an even numbered address. If an interface controller develops multiple interrupts, the base addresses of these interrupts are partitioned either two or four locations apart. The standard base addresses are : 0XX2, : 0XX6, : 0XXA and : 0XXE. These standard base addresses leave locations : 0XX0 and : 0XX8 available for special interrupts, if required.

The Auto I/O instruction requires three locations while the IMS and JST instructions require one location each. The unused reserved locations may be used for address pointers.

5.4.2 Single Interrupt Implementation Using IUR- (Figure 5-7)

This structure features an Interrupt Enable flip-flop (INTE), an Interrupt Stimulus Store flip-flop (INTS), an Interrupt Pending flip-flop (IP1), priority determination logic, priority out disable logic and an interrupt address generator.

The INTE flip-flop is a J-K type device which is synchronously set or reset by an addressed select command. Function code M (FCM) sets INTE while function code R (FCR) resets INTE. The INTS flip-flop is a D-type positive-edge triggered circuit. When enabled, INTS sets on the positive excursion of the external stimulus signal (EXTS).

An optional feature is an edge detector consisting of an Exclusive-OR gate and an inverter. The edge detector permits the use of either a high or low stimulus signal. The polarity of EXTS is defined by RPOL (Request Polarity). If EXTS is a low signal when active, RPOL is grounded. Likewise, if EXTS is a high signal when active, RPOL is left open and the pull-up resistor provides the positive-logic level signal. When both EXTS and RPOL are of the same polarity, the output of the edge detector will be high causing INTS to set, if enabled. Once both INTE and INTS are set, an interrupt request is generated. The Interrupt Pending flip-flop is enabled when INTE and INTS are both set. When enabled, IP1 sets on the negative excursion of the Processor I/O clock (IOCL).

Once IP1 is set, the structure must have priority before an IUR interrupt request can be generated. If up-stream devices are not generating interrupts, PRIN- (priority in, pin 83) will be low. Both PRIN and IP1 are ANDed to produce the interrupt request signal, ME. ME is used to develop the IUR- signal and disable down-stream interrupts by causing PROT- (priority out, pin 84) to go high.

When the Processor recognizes the interrupt request, it responds by issuing the interrupt address request (IAR). If ME is still high (a higher priority interrupt may have been generated at the same time as this one, causing PRIN- to go high, disabling ME), IAR causes the interrupt address to be generated.

The interrupt address generator develops a unique vectored interrupt address. The base address that is developed is : 0XX2. The Interrupt Address Select lines (E4- through E256-) permit the user to displace the base address anywhere in the first 512 words of memory. Grounding a particular address select line adds a corresponding decimal value to all base addresses. For example, grounding E32- adds 32 decimal locations to all interrupt addresses.

This type of address generation permits the user to re-define interrupt locations with a minimum of effort. In the event the user is limited by the number of pins available, specific data bus drivers can be used instead of the structure shown.

When ME and IAR are high (ADRR), the data bus drivers are enabled and the interrupt address is transferred to the Processor. The Processor directs the contents of the data bus to the memory address register. After the memory address register is loaded, the PLSE signal is generated. The PLSE signal, NANDed with ADRR, will cause INTS to reset.

At the end of the last cycle of the interrupt instruction, IOCL is re-enabled. With INTS reset and IOCL enabled, IP1 resets on the negative excursion of IOCL terminating the IUR interrupt request.

The only feature of the interrupt structure not mentioned previously is the initialize feature. Generally all interface controllers have an initialize circuit which generates the INZ signal. INZ sets or resets all control flip-flops to a known condition. In this case, INTE and INTS are reset by INZ. INZ is typically generated in response to an addressed Select command with function code 4 or by the Processor generated System Reset signal, RST-.

5.4.3 Echo Interrupt Implementation Using IUR (Figure 5-8)

The interrupt structure shown in figure 5-8 develops two interrupts on the IUR- request line.

The structure is similar to the IUR structure described in paragraph 5.4.2 except than an Echo Interrupt flip-flop (ECHOI) is added. The interrupt request is developed as a result of ORing IP1 and ECHOI, and two base addresses are developed (: 0XX2 for IP1 and : 0XX6 for ECHOI).

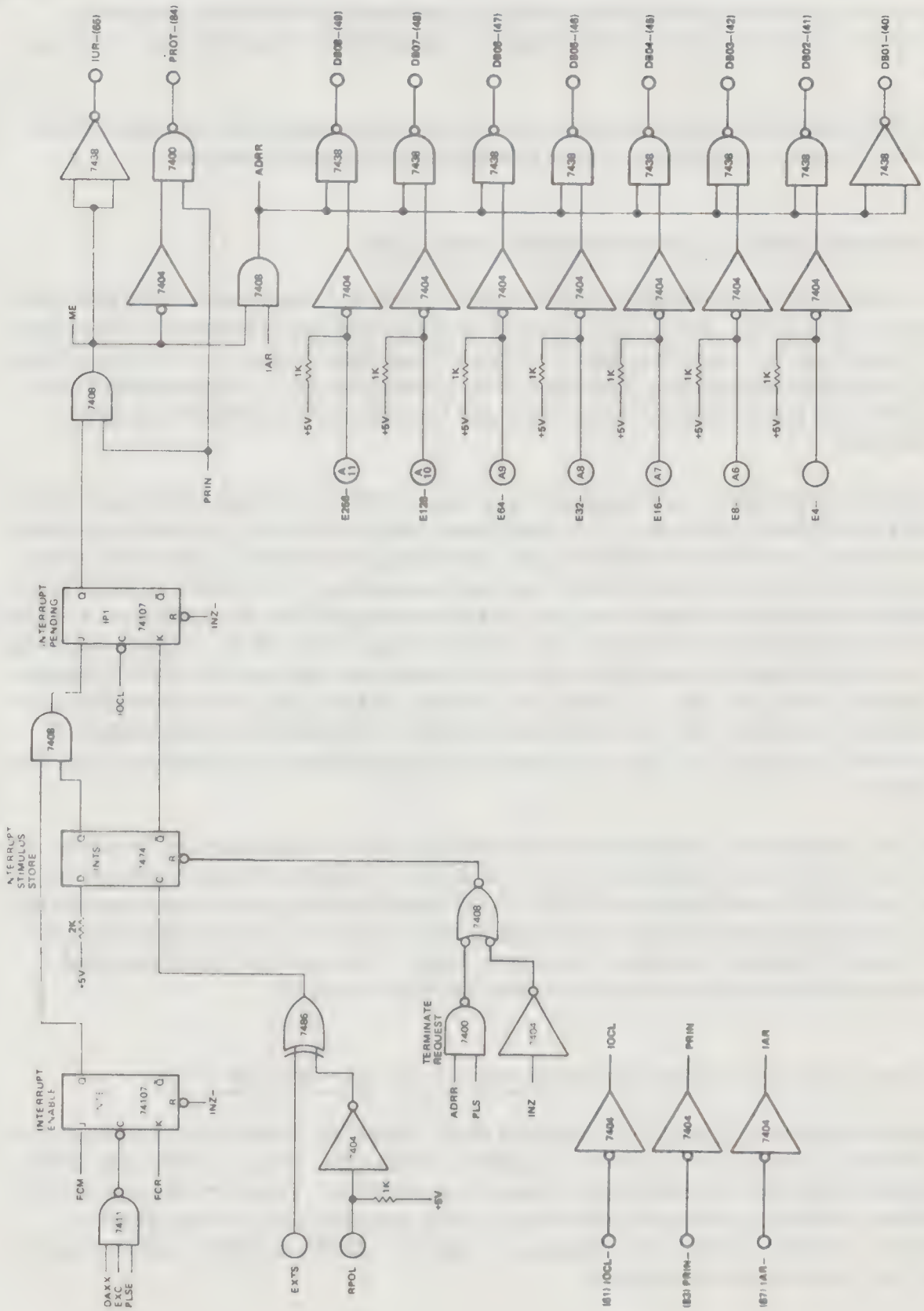


Figure 5-7. Single Interrupt Implementation Using IUR-

ECHOI is enabled by IP1 and PRIN. If the structure has priority at the instant an ECHO is developed by the interrupt instruction, ECHOI sets when the ECHO is received. ECHOI is reset, if IP1 is reset, if the structure has priority when IAR and PLSE are received.

Note that IP1 is set for the entire period of the interrupt instruction and that ECHOI is set only as long as required to obtain recognition from the Processor.

5.4.4 Reentrant Interrupt Implementation (Figure 5-9)

Reentrant interrupt programming permits an interrupt of higher priority to interrupt an interrupt subroutine. Interrupts of lower priority are not recognized. Reentrant interrupt programming requires that the Priority Out Disable latch be implemented in the user's interface hardware. When the latch is implemented, the generation of an interrupt sets the latch which in turn, disables the generation of PROT- to downstream devices.

The reentrant interrupt feature disables all lower priority interrupts for the duration of an entire interrupt subroutine. The reentrant interrupt circuit is shown in figure 5-9. The circuit prevents the PROT signal from being transmitted to the next lower priority controller until the subroutine has been completed. The PROT disable latch is initially set when the interrupt request is acknowledged with the Interrupt Address Request (IAR) signal from the Processor. IAR is ANDed with ME to produce Address (ADRR) which enables the interrupt address drivers and also sets the PROT Disable latch. PROTD- thus goes low, disabling the 3-input NAND gate which normally produces the PROT- signal when ME- goes false (high). Inhibiting the generation of PROT- prevents priority from being passed on to lower priority controllers until the latch is reset.

The latch can be reset by issuing a Select command with a function code dedicated to resetting the latch, or by initializing the controller. When the Select command is decoded, the DEXP (combination of DAXX, EXEC and PLSE signals) signal goes high. DEXP is NANDed with the appropriate function code (FCX) and is applied through a negative input OR gate to the reset side of the latch. The latch is thus reset and PROT- is passed on to lower priority devices (if PRIN- is low).

5.4.5 Single Interrupt Implementation Using IL1- or IL2- (Figure 5-10)

The structure shown in figure 5-10 consists of an Interrupt Enable and an interrupt request driver. The interrupt enable is used to enable the driver. When the external stimulus is applied, an interrupt request is generated. This structure demands that the external stimulus remain active until some positive action takes place to move data or transfer control (the issuance of the IN-, OUT- or EXEC- control signals with the proper device address).

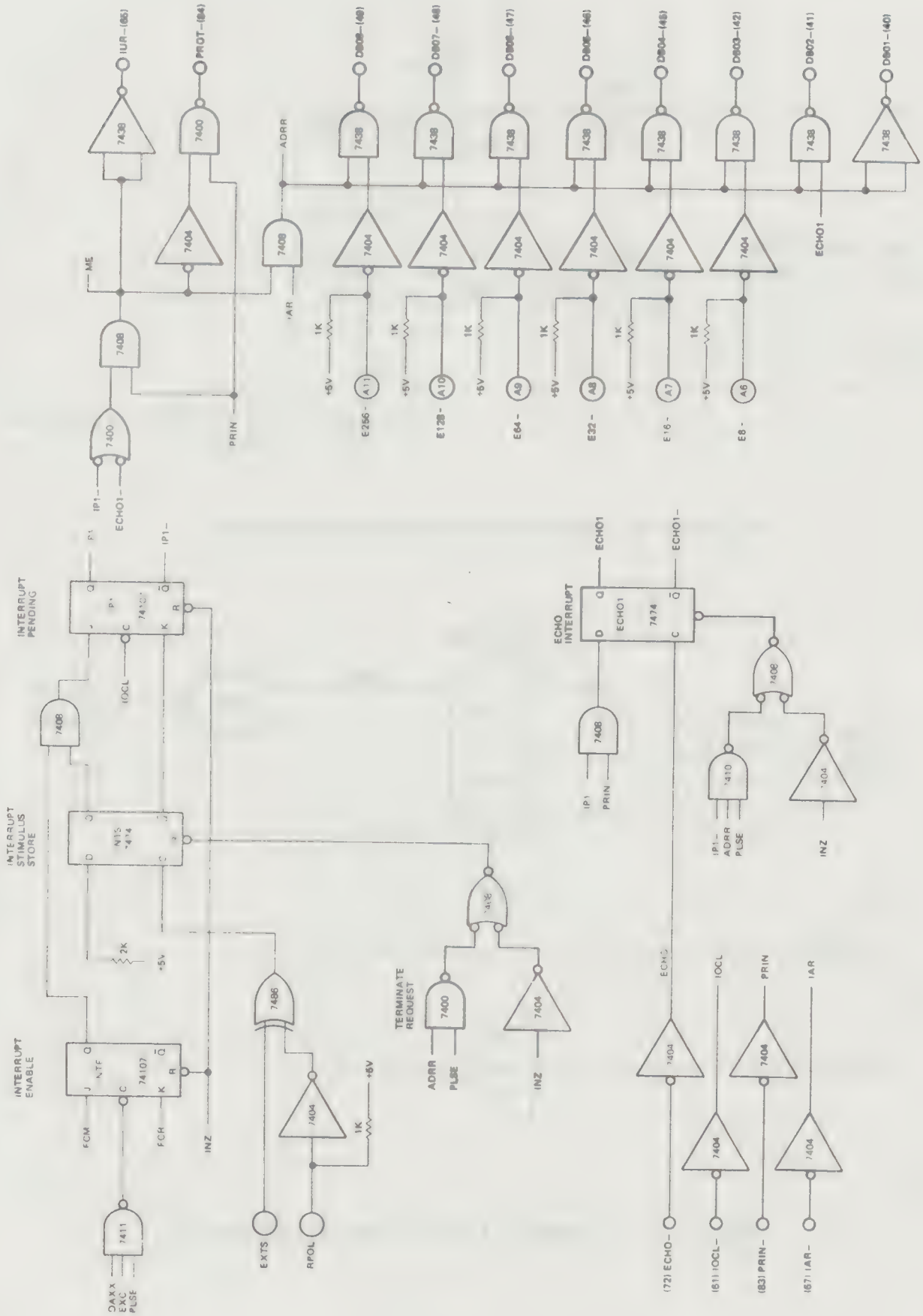


Figure 5-8. IUR- Echo Interrupt Implementation

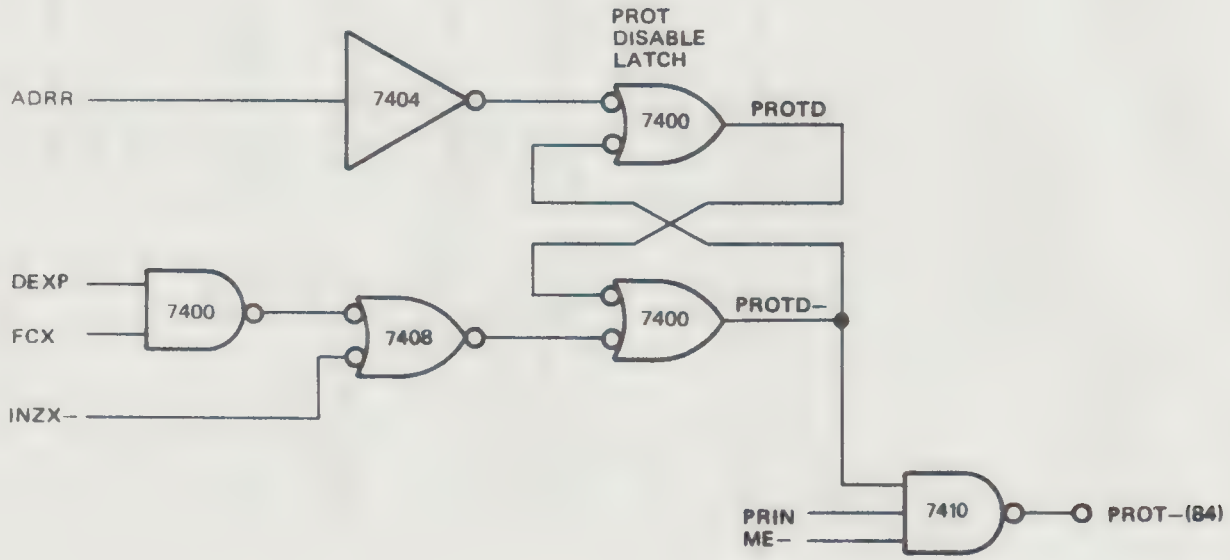


Figure 5-9. Reentrant Interrupt Implementation

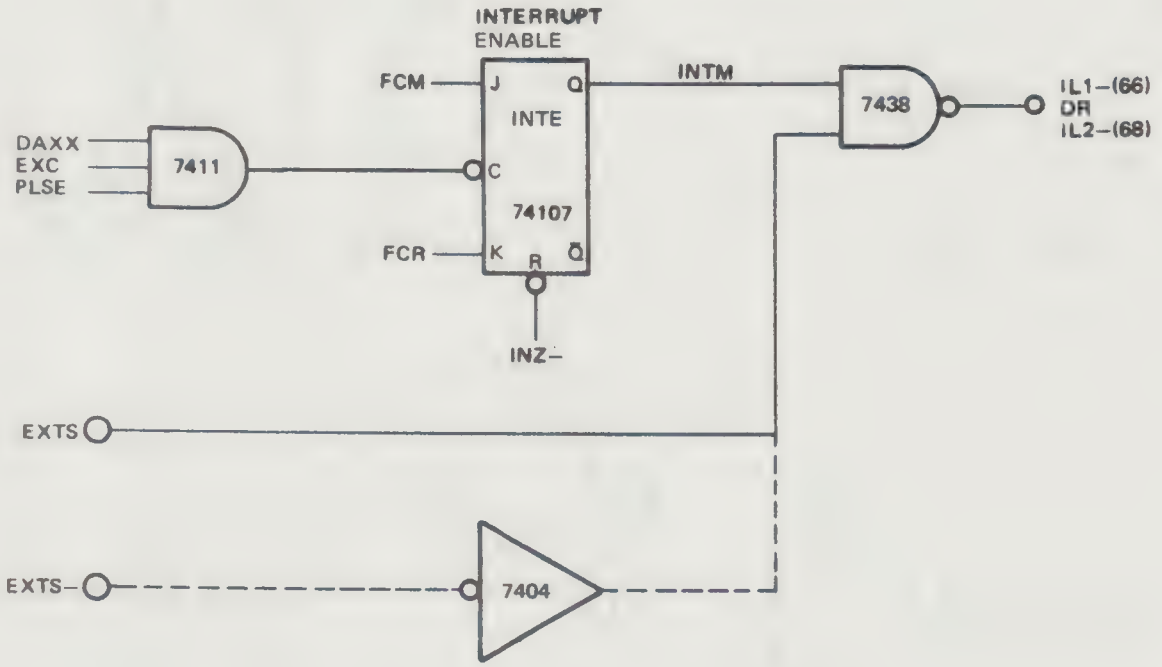


Figure 5-10. Simple IL1-/IL2- Interrupt Structure

5.4.6 Echo Interrupt Implementation Using IL1 and IL2 (Figure 5-11)

The interrupt structure shown in figure 5-11 develops two interrupts which utilize the IL1- and IL2- request lines. Since this interrupt structure is designed to accommodate any echo generating instruction (the four Auto I/O instructions and the IMS instruction), no other devices may be attached to the IL1- and IL2- request lines. These lines are totally dedicated to this structure.

This structure is essentially the same as the IUR- structure described in paragraphs 5.4.2 and 5.4.3. The most significant difference is that the request flip-flops are distributed directly to the IL1- and IL2- drivers. The operation of this structure is essentially the same as the IUR structures, except during request termination. Once the interrupt request is generated, the request must be recognized by the Processor. The Processor recognizes the highest priority interrupt first and all other requests in their order of priority. Since there are four higher priority interrupts above IL1 (power fail, trap, console interrupt and memory parity) and five above IL2- (the four just mentioned and IL1), the interrupt structure must be able to detect no higher priority interrupt activity before terminating the request. The only thing that the power fail, trap, console interrupt and memory parity interrupts have in common is that during the interrupt address request interval, they all cause bit 4 of the Data bus to be low. If DB04- is low during IAR, the IL1 request will not reset but will remain active since the Processor has not honored the request. When no higher priority exists after generating the interrupt request, INTS is reset on the leading edge of the PLSE signal and terminates the interrupt request. To avoid re-triggering the INTS flip-flop, the interrupt stimulus should remain in the active condition until an addressed I/O command (Select, Input or Output) causes the source of the stimulus to reset.

5.5 PRIORITY PROPAGATION

It is the users' responsibility to propagate interrupt priority, regardless of whether or not an interface controller develops interrupts. If an interface controller does not develop interrupts, the PRIN- and PROT- signals must be jumpered together inside the interface controller.

Interface controllers that develop IUR interrupts should use TTL gates for unloading PRIN- and driving PROT-. It is imperative that the propagation delays internal to the interface controller be minimized. A total of two microseconds is allowed for priority propagation through all controllers in a chain. The implementation of expansion chassis Buffer Card look-ahead propagation limits the longest priority propagation path to the maximum number of controllers that can be installed in two chassis (20 controllers). Priority propagation delays should therefore be held to less than 100 nanoseconds average per controller.

5.6 I/O BUS LOADING RULES

In order to conserve the I/O bus drive capability of the Processor, an interface should not present more than one load (1.6 ma typical) to any given I/O bus signal. If the interface controller presents more than one load to a given signal, the user should unload the signal upon entry into the interface.

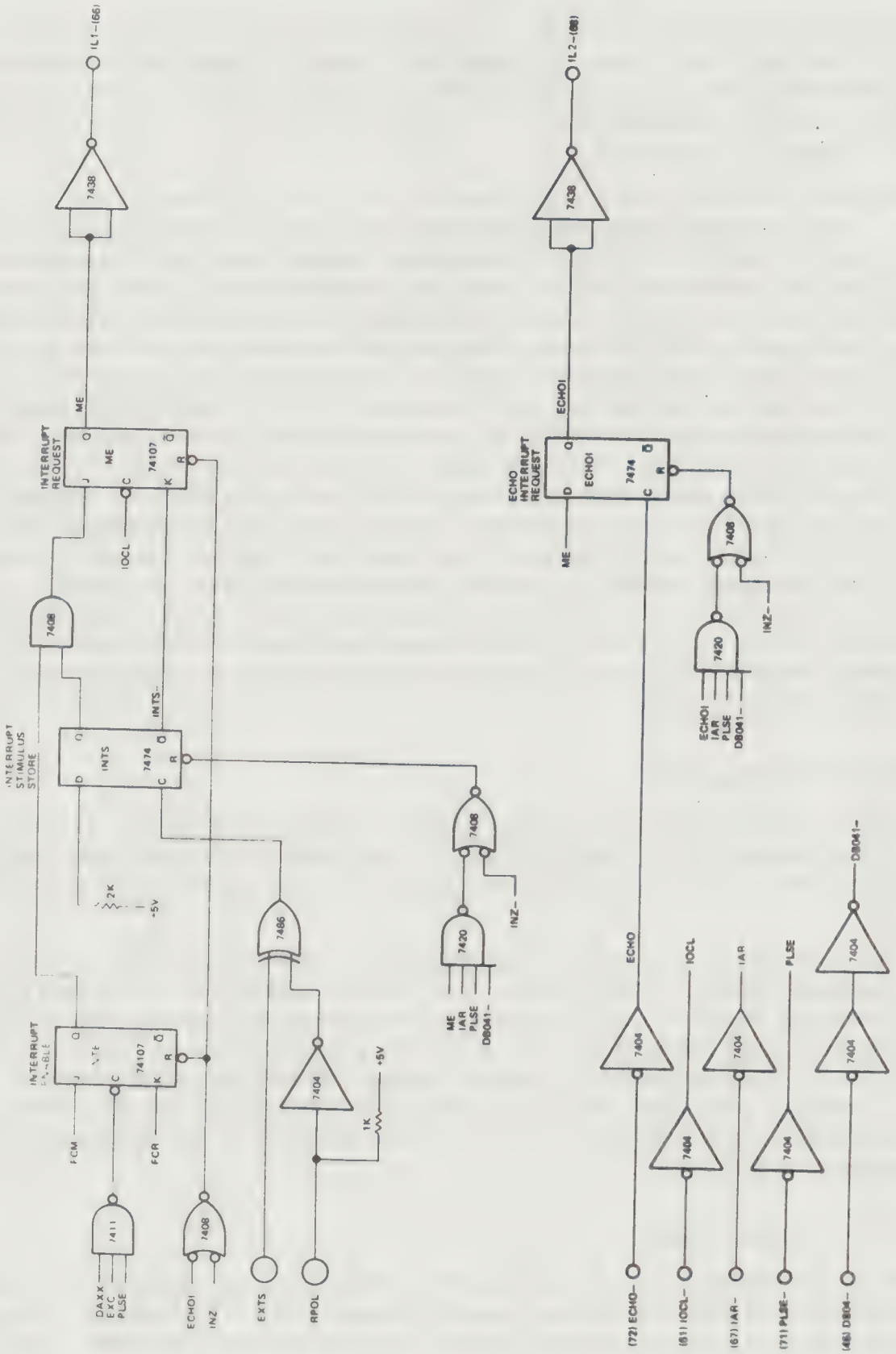


Figure 5-11. Echo Interrupt Implementation Using IL1- and IL2-

5.7 POWER AND GROUND SYSTEM CONCEPTS

The power supply that is furnished with the ALPHA 16 LSI computer produces three voltages: +5Vdc, +12 Vdc and -12 Vdc. The +5 volt supply is used to provide the VCC voltage for all integrated circuits in the Processor, Memory and I/O modules. The +12 and -12 volt supplies are used by the Processor and Memory modules and are available to all I/O modules if needed. Typically the +12 and -12 volt supplies provide power for analog and communications type interfaces. All three regulated voltages share a common ground system referred to as logic ground.

Power (+5, +12 and -12 Vdc) and logic ground are distributed from the system power module through the motherboard to all plug-in modules. Within a module, +5V and ground are distributed by means of bus bars. The power and ground pins on the motherboard are organized such that each bus bar can pick up a separate set of pins.

A typical half card module has a density of 72 integrated circuits which are organized in six rows of 12 chips. A typical full card module has a density of 144 IC's organized in 12 rows of 12 chips. Bus bars are mounted in between each row of chips and on the outside edges of a card. A half card module has seven bus bars while a full card module has 13. Odd numbered bus bars are ground, even numbered bus bars are +5 Vdc.

Most 14-pin chips use pin 14 for Vcc (+5 Vdc in this case) and pin 7 for logic ground. A typical 16-pin chip uses pin 16 for Vcc and pin 8 for logic ground. By alternating the pin 1 orientation of each row of chips, two rows of chips can share a common +5 or ground bus bar. All bus bars are approximately 14 inches long and have 24 pins located on .6 inch centers. The Vcc pins of all chips in adjacent rows are routed to the nearest +5 bus bar mounting pad. Likewise, all ground pins in adjacent rows are routed to the nearest ground bus bar mounting pad.

The bus bar is designed such that when it is installed there is a .075 inch gap between the underside of the bus bar and the printed circuit board. This is to permit etched circuitry to pass underneath the bus bar without shorting.

Table 5-1 lists all power and ground pin assignments that exist in the 100 and 200 connectors of a typical motherboard slot.

Table 5-1. Power and Ground Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
1,2	Ground	43,44	+5 Vdc
3,4,5,6	+12 Vdc	59,60	Ground
7,8	-12 Vdc	73,74	+5 Vdc
13,14	+5 Vdc	85,86	Ground
27,28	Ground		

There are two ground systems in the ALPHA 16 LSI computer. They are logic ground and chassis ground. It is recommended that the user avoid tying these two ground systems together. The chassis ground system usually has more noise than the logic ground system can tolerate. In the event it is necessary to tie the two systems together, they should be tied together at only one point in the users' system. For personnel protection, the chassis ground system is tied to earth-ground via the third wire in the AC line cord.

5.8 FILTERING TECHNIQUES

Integrated circuits introduce switching transients into the +5 Vdc power supply which must be filtered out. It is recommended that both high frequency and low frequency filtering be employed. The low frequency filter consists of a 2.2 microfarad, 10 per cent, 20 Vdc tantalum capacitor between +5V and ground for each row of 12 chips. The high frequency filter consists of a .022 microfarad, 25 Vdc ceramic capacitor between +5V and ground for every four chips in a given row of chips. Thus a typical half card module would have 6 tantalum capacitors and 18 ceramic capacitors for transient filtering. Where a large number of MSI devices and Fairchild 9602 one-shots are used, it is recommended that a .022 microfarad ceramic capacitor be used for each device.

The -12 Vdc supply is used by the inhibit drivers in memory. The inhibit drivers introduce approximately .5 volts of transient noise into the -12 Vdc power supply. If the user cannot tolerate this much noise, an inductive input type filter is recommended.

5.9 STANDARD INTERFACE CONNECTOR

The standard interface connector is a Viking 3VH50/1JN5 or equivalent. This connector features two rows of 50 contacts designated A1 through A50 and B1 through B50. Contacts A1 through A50 interface with the contact strip on the solder side of the printed circuit board. Contacts B1 through B50 interface with the component side of the board. The interface connector should be installed with pins B1 and A1 to the left as viewed from the rear of the computer.

5.10 NORMAL INTERFACE PINS

The interface pin assignments normally used by CAI for device address and interrupt address jumpers are listed in Table 5-2.

Table 5-2. Normal Interface Pins

PIN	SIGNAL	PIN	SIGNAL
A01	PS4-	B01	+5Vdc
A02	PS3-	B02	+5Vdc
A03	PS2-	B03	Ground
A04	PS1-	B04	Ground
A05	PS0-	B05	Ground
A06	E8-	B06	Ground
A07	E16-	B07	Ground
A08	E32-	B08	Ground
A09	E64-	B09	Ground
A10	E128-	B10	Ground
A11	E256-	B11	Ground

Section 6

DMA DESIGN REQUIREMENTS

6.1 INTRODUCTION

The ALPHA LSI computer has a direct memory access post (DMA) which permits specially built controllers (referred to as DMA controllers) to transfer data via the Maxi-Bus at very high speed to or from memory or other controllers.

6.1.1 Maxi-Bus Characteristics

The Maxi-Bus consists of 58 lines (plus power and ground) that are used to convey address, data and control information to or from the Processor, DMA Controllers, Memory and I/O contollers.

The Maxi-Bus provides a common transfer path for all system modules. Maxi-Bus transfers involving memories are asynchronous wherein the amount of time that signals from a source device spend on the Maxi-Bus depends upon the access and cycle time of the addressed memory and not upon a fixed clock interval. All Maxi-Bus operations between the Processor and Input/Output controllers are synchronous and therefore do not require timing generation within I/O controllers.

All address and data signals as well as memory control signals from a source device must be driven 32 mA tri-state drivers. Certain control signals that can be driven simultaneously by more than one device must use 32 mA open-collector drivers. Standard TTL receivers can be used by all devices. Only one receiver per line per module is permitted and the maximum receiver loading must not exceed 1.8 mA per module.

Address and data lines are shared by memories and I/O devices. During communication intervals involving memories, all bus drivers on these lines must be tri-state. During communication intervals involving standard I/O devices, bus drivers may be either tri-state or open collector.

6.1.2 Processor Provisions

The ALPHA LSI Processor is designed to surrender the Maxi-Bus to a DMA controller whenever a stop command (STOP-) is received. Upon receipt of the STOP- signal, the Processor completes the current microcycle, stops and sends a stop acknowledge signal (SACK-) to the requesting DMA controller(s).

A DMA controller may generate STOP- at any time and keep the signal active for any length of time. The SACK- signal will remain active as long as STOP- is active.

6.1.3 Memory Operations

DMA controllers may communicate directly with memory. The DMA controller must emulate the Processor by generating a memory address and appropriate control signals. Memory operations may be either read (data accessed from memory) or write (data written into memory). Data can not be read, modified and rewritten in one cycle. When communicating with a single memory, data transfer rates of up to 625,000 words per second can be achieved with the standard 1.6 microsecond memories. When more than one memory module is used in the computer, DMA transfer rates of up to twice the basic speed of the memory can be achieved by making alternate memory accesses in different modules. Memory interleaving straps allow even and odd addresses to be in separate memory modules so that sequential addressing automatically alternates between modules.

In addition to word transfer capabilities, byte transfers may be performed by a DMA controller. All byte packing and unpacking is done automatically by the memories with all byte data transferred on the lower eight data bus lines (the upper eight data bus lines are ignored during byte transfers).

All memories contain data and address registers to permit asynchronous operation. During a write operation, the source device furnishes an address and data along with a memory start signal. As soon as the address and data is stored in its registers, the memory issues an acknowledge signal and releases the bus even though it has not actually finished the write operation. During a read operation, the memory accesses the addressed location, places the data on the D bus and then issues the memory acknowledge signal. When the source device recognizes the memory acknowledge signal, it removes the start signal releasing the Maxi-Bus. Any memory restore operation or overhead interval does not tie up the Maxi-Bus and therefore the Processor or a DMA controller is free to perform another operation.

6.1.4 I/O Operations

A DMA controller may emulate the I/O instructions of the Processor. The DMA controller may issue Input, Output, Sense, Select, and Select and Present commands. It may perform conditional and unconditional I/O. All I/O command and control lines of the Maxi-Bus that are used by the Processor for I/O operations are available to a DMA controller when the Processor is stopped.

6.1.5 Limitations

A DMA controller is not permitted to use the interrupt processing capabilities of the Processor. Interrupts are reserved for use by the Processor only. I/O controllers that are under control of a DMA controller must have their interrupt facilities disabled.

When multiple DMA controllers are employed in a system, they must compete for control of the Maxi-Bus on a priority basis. DMA Priority lines are strung serially through the 200 series connectors of the ALPHA LSI motherboard. Therefore, DMA controllers must be either full cards or half cards that are installed in the 200 series connectors of the ALPHA LSI motherboard.

When using the standard expansion chassis buffer card, a DMA controller must be in either the same chassis or in a chassis that is closer to the Processor than a memory or I/O controller that it must communicate with. This is because the expansion buffer card treats unidirectional lines (such as the A bus lines) as originating from the Processor end of a chain of expansion chassis. Therefore unidirectional signals which normally originate from the Processor cannot be transmitted to an upstream memory or I/O controller.

6.2 DMA TIMING

The following paragraphs define DMA transfer timing. All timing intervals shown in timing diagrams are in nanoseconds and all timing intervals discussed in the text are nominal. Times determined by memory access and cycle intervals are shown for the standard 1.6 microsecond memory and may be different for other types of memories.

6.2.1 Maxi-Bus Acquisition Timing (Figure 6-1)

Two signals are involved with Maxi-Bus acquisition: STOP- and SACK-. When a DMA controller is ready to make a transfer it drives the STOP- line low (ground-true). The Processor upon seeing STOP- low, immediately begins preparing to vacate the Maxi-Bus. After performing the required internal housekeeping associated with stopping. the Processor drives the Stop Acknowledge (SACK-) signal low (ground-true). The time interval from the leading edge of STOP- to the leading edge of SACK- can be as much as 4800 nanoseconds for the Type 1 Processor.

Once SACK- goes low, the DMA controller is free to commence transfer operation. Typically, DMA controllers operate on a request basis wherein they make one transfer for each request received from an associated peripheral. If the DMA controller receives another request prior to completion of the current transfer (burst mode), it will keep STOP- active, otherwise it releases the STOP- line when the current operation is completed.

After releasing the STOP- line, the DMA controller may not attempt to reacquire the Maxi-Bus before SACK- goes high. The Type 1 Processor can take up to 2400 nanoseconds to raise SACK- and restart programmed operation. Once SACK- goes high, the DMA controller is forced to wait out the DMA acquisition period before acquiring the Maxi-Bus again. Therefore, the worst case latency period is 5600 nanoseconds for the Type 1 Processor. The Type 2 Processor DMA latency is a function of the type of memory used. The Type 2 Processor DMA latency times are as follows:

Core 980 = 1405 nanoseconds
Core 1200 = 1825 nanoseconds
Core 1600 = 2575 nanoseconds
SC 1200 = 3025 nanoseconds

Latency time may be longer if a higher priority DMA controller is also requesting the Maxi-Bus.

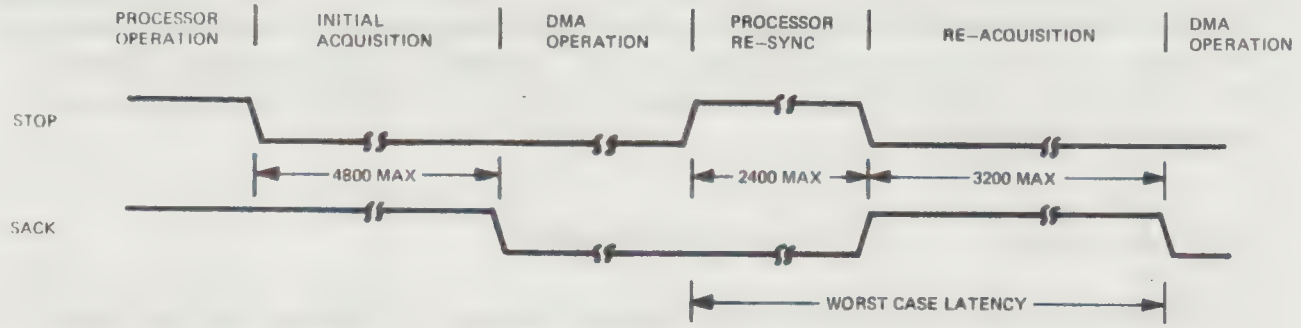


Figure 6-1. Maxi-Bus Acquisition Timing

6.2.2 Memory Transfer Timing (Figure 6-2)

Memory modules of various speeds, sizes and technologies may be intermixed in a system. The standard 4K core memory has a cycle time of 1600 nanoseconds which provides a maximum data transfer rate of 625,000 words/bytes per second.

A memory cycle is divided into an access interval and an overhead interval. The access interval is the period when data is transferred to or from memory. The overhead interval is used for internal memory operations. For core memories the overhead interval is used to restore the contents of the word just read or to write the word just transferred. For non-destructive readout memories, the overhead interval consists primarily of logic recovery time. For dynamic MOS memories, the overhead also includes cycles stolen by memory to refresh dynamic storage. During the overhead interval, the Maxi-Bus is available for other operations.

For DMA applications requiring data transfer rates in excess of 625,000 words/bytes per second, memory interleaving can be employed. When alternate memory cycles address different memory modules, each memory's overhead interval can be used to access another memory, yielding transfer rates up to twice that possible with a single memory. Each memory module features static control lines at the rear of the module which permit the memory module to operate in the interleaved mode. Each memory module can be configured to respond to either even or odd memory addresses. This feature allows sequentially addressed memory locations to automatically alternate between memory modules.

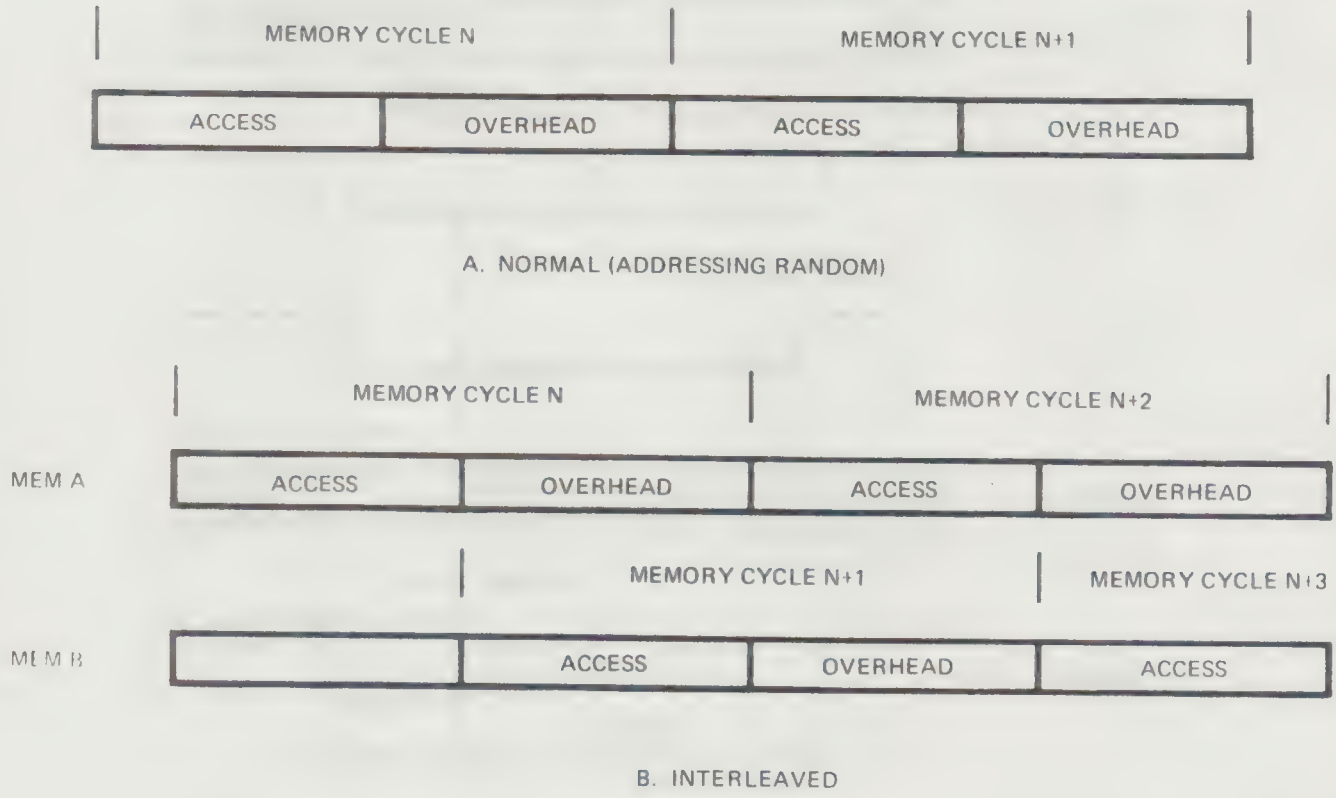


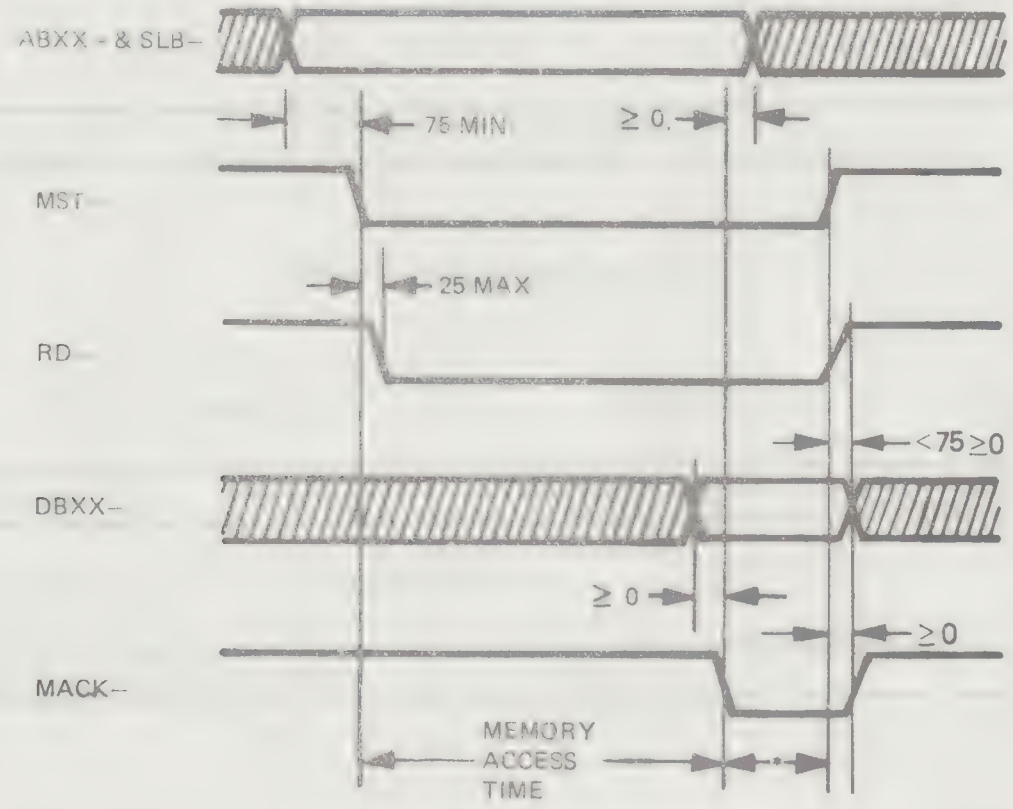
Figure 6-2. Memory Addressing Comparisons

6.2.2.1 DMA Read Access Timing (Figure 6-3)

A DMA read access sequence is started by the DMA controller placing the desired memory address on the A bus. A minimum of 75 nanoseconds is required for A bus settling and address recognition for all memories before the DMA controller drives the Memory Start signal (MST-) low. The Read signal (RD-) must be driven low no later than 25 nanoseconds after MST- goes low.

The addressed memory begins execution of a memory cycle when MST- goes low, and after it has finished any previous operation. When the addressed location has been accessed (approximately 450ns for standard 1600ns memories), the contents of the addressed memory location are placed on the D bus and a Memory Acknowledge signal (MACK-) is issued. The information of the D bus will remain stable until MST- is removed.

Upon receipt of MACK-, the DMA controller is free to disengage the A bus. After allowing for settling time on the D bus, the DMA controller stobes the contents of the D bus into a receiving register and removes MST- and RD-. The memory module removes MACK- on the trailing edge of MST- and disengages the D bus on the trailing edge of MST- or RD-, whichever goes away first. The DMA controller must disengage the A bus prior to or coincident with removal of MST-. The DMA controller may not initiate another memory cycle until MACK- has been removed.



* INTERVAL DETERMINED BY CONTROLLER TO ACCEPT MEMORY DATA

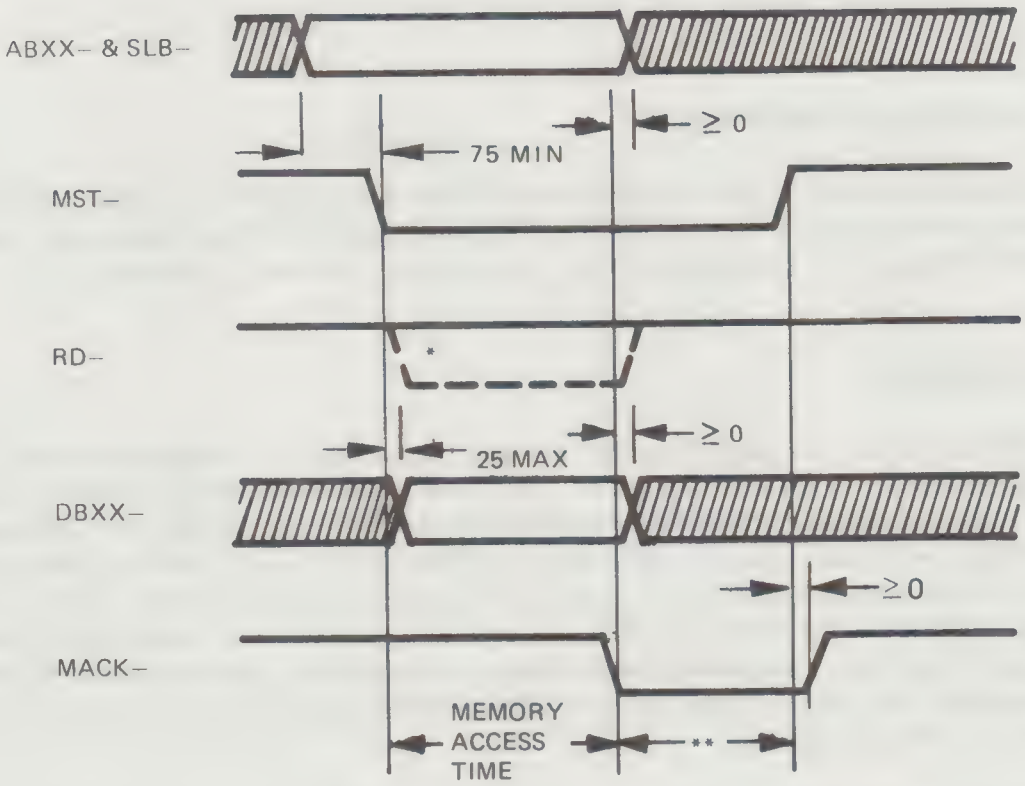
Figure 6-3. Read Access Timing

6.2.2.2 DMA Write Access Timing (Figure 6-4)

A write access sequence is similar to a read access sequency except that the RD- signal is held high and the write data is presented to the addressed memory at the same time MST- is generated.

A write access is started by placing the memory address on the A bus. After a minimum of 75 nanoseconds the Memory Start signal is driven low. The RD- signal is held high and the write data is gated onto the D bus no later than 25 nanoseconds after MST- goes low. The memory indicates acceptance of the write data by driving the MACK- signal low.

The DMA controller must disengage the A bus and the D bus and remove MST- when MACK- goes low. MACK- is removed on the trailing edge of MST- at the memory.



* RD– may be forced low by memory protect option to abort write cycle

** controller may remove MST– as soon as MACK– is recognized

Figure 6-4. Write Access Timing

6.2.3. I/O Transfer Timing

A DMA controller may transfer data to or from another controller by emulating the Processor's operations on the I/O control signals. I/O Transfer timing is discussed in detail in Section 2 of this manual.

A single exception to standard I/O transfer sequencing involves generation of MACK during I/O transfers under DMA that do not involve the use of memory. In this case the DMA controller must generate MACK- for a minimum of 100 nanoseconds prior to completion of the I/O transfer. This allows other DMA controllers in the system to synchronize any pending Maxi-Bus requests and properly auction DMA priority (see paragraph 6.3.2.2).

6.3 OPERATIONAL OVERVIEW

DMA controllers generally have three basic phases of operation. These phases are initialization, execution, and termination. This section provides a general overview of each of these phases. A simple overview flow chart is shown in figure 6-5.

6.3.1 Initialization

The initialization phase is used to transfer task parameters from an operating program to the DMA controller. Typically, the task parameters define operating modes, data transfer paths, the total number of transfers to be made, the starting memory address (if memory is involved) and search parameters for items such as a disk or tape unit. The complexity of the task parameters is directly related to the complexity of the DMA controller and the various tasks it can perform. Depending on the DMA controller design, the task parameters can be transferred from memory to the DMA controller's registers either by use of normal I/O instructions or by means of a task control block which is read from memory by the DMA controller.

Once the task parameters have been transferred, the DMA controller may begin data transfer execution.

6.3.2 Execution (Figures 6-6 through 6-8)

The execution phase is entered upon completion of initialization. When the associated peripheral logic is ready to transfer data, it generates a DMA transfer request. The DMA controller executes the DMA request in three stages. These stages are Maxi-Bus acquisition, priority auction, and data transfer. Figure 6-6 shows a typical implementation of the Maxi-Bus acquisition and priority auction logic. Figure 6-7 shows the state counter and decoder implementation. Figure 6-8 depicts the timing for both a memory write and memory read operation.

6.3.2.1 Maxi-Bus Acquisition

Maxi-Bus acquisition is initiated upon receipt of a data transfer request. The Maxi-Bus acquisition logic consists of three control elements: a Request Store flip-flop (RQ), a Request Sync flip-flop (REQF) and a STOP- driver.

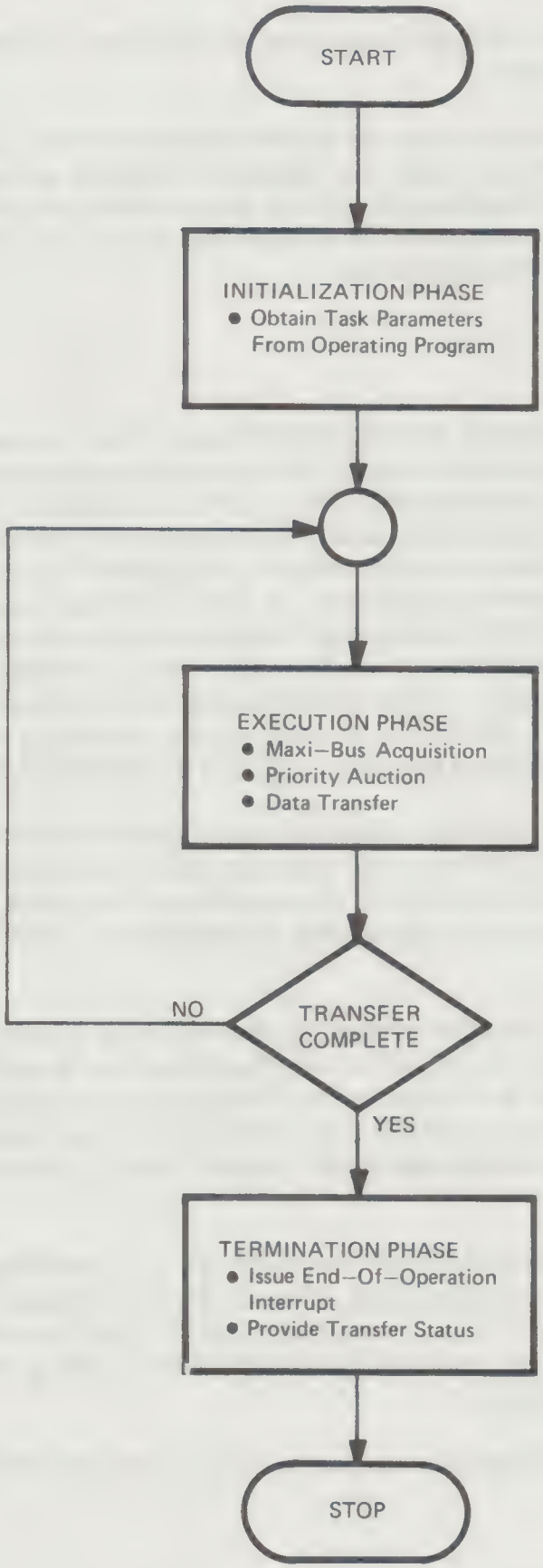


Figure 6-5. DMA Operational Phases

The data transfer request is stored in the Request flip-flop. RQ remains set until the data transfer stage is entered.

If no DMA operations are currently in progress (Processor Stop Acknowledge signal, SACK-, high), the Request Sync flip-flop is asynchronously set which causes STOP- to go low requesting use of the Maxi-Bus. If a DMA operation is in progress (SACK- low), the Request Sync flip-flop must be set synchronously with Memory Acknowledge (MACK-) to assure proper bus operation.

6.3.2.2 Priority Auction

Priority auction is required only if multiple DMA controllers are employed in the same system. Priority auction permits multiple DMA controllers to compete for use of the Maxi-Bus by means of the DMA priority string (DPIN- and DPOT-). DPIN- is the name given to the priority chain as it enters a controller and DPOT- is the name given to the priority chain as it leaves each controller. The DPOT- of one controller is the DPIN- of the next lowest priority controller. A DMA controller has priority if its DPIN- line is low. The number of DMA controllers which may be used within the system is limited only by priority ripple time on the priority string. Nominally 200 nanoseconds are allocated to priority ripple. Where more than 200 nanoseconds is required for priority ripple, each DMA controller must be designed to abstain from beginning a transfer operation until sufficient time has elapsed for priority ripple.

Priority auction occurs at two times: after the leading edge of SACK- and, if another request has been received, after the data transfer (after the trailing edge of MACK-). If only one DMA controller is installed in the system or if only one DMA controller is allowed to be active at a time in multiple DMA configurations, then priority ripple time need not be allocated.

Within the DMA controller, priority auction is controlled by a DMA Start flip-flop (START). START is enabled by REQF (which indicates that a synchronized data transfer request is pending) and is clocked by the leading edge of SACK- during initial Maxi-Bus acquisition or by the trailing edge of MACK- during sequential DMA operations. When set, START inhibits downstream DMA Priority (DPOT-, high) and starts the DMA state counter.

When two or more DMA controller START controls are set simultaneously, the highest priority controller inhibits priority to the downstream controllers. The downstream controllers upon seeing DPIN- high, reset their START flip-flop and DMA state counter aborting the data transfer. An aborted transfer remains pending until all higher priority DMA requests have been serviced.

Priority auction terminates when the auction interval (normally 200 nanoseconds) has been timed out.

6.3.2.3 Data Transfer

When the data transfer interval is entered, the DMA controller is free to initiate data transfers to or from memory or another I/O controller. All data transfer timing is controlled by the DMA controller per paragraph 6.2.2 for memory transfers and per Section 3 for transfers to/from another I/O controller. For each data transfer, the DMA controller must generally decrement a word or byte counter and increment an address counter if transferring data to/from memory. These overhead operations generally take place immediately after a data transfer to assure that address information is stable during the next data transfer. When a data transfer is completed, the DMA controller enters the Priority Auction stage if more data transfers remain or enters the termination phase if all transfers are complete.

6.3.3 Termination

A DMA controller should provide for two types of termination: normal and abnormal. A normal termination occurs when the transfer counter decrements to zero with no errors detected. An abnormal termination occurs if an error condition exists. Since DMA transfer operations can be terminated for a variety of reasons, termination flags should be used to store the reason for a termination.

When a termination condition exists (either normal or abnormal) subsequent DMA transfer requests are inhibited, Maxi-Bus control is returned to the Processor, and an end-of-operation interrupt is developed by the DMA controller. In some cases, it may be desirable to have the Processor periodically examine DMA controller status rather than generate a termination interrupt.

Typically, the end-of-operation interrupt service routine will input the termination flags and any other pertinent status and determine if the complete transfer was acceptable. If the data transfer was not acceptable, the software may retry the transfer operation if it deems it necessary.

It is the responsibility of all DMA controllers to terminate with the current bus operation and not request further bus operations in the event of a power failure (PFD-low). This is necessary to allow the Power Fail/Restart circuitry to interrupt the Processor so that a software power down subroutine can be executed. Normally a DMA controller will set a termination flag in the event of a power failure during operation so that software will be aware of an incomplete operation.

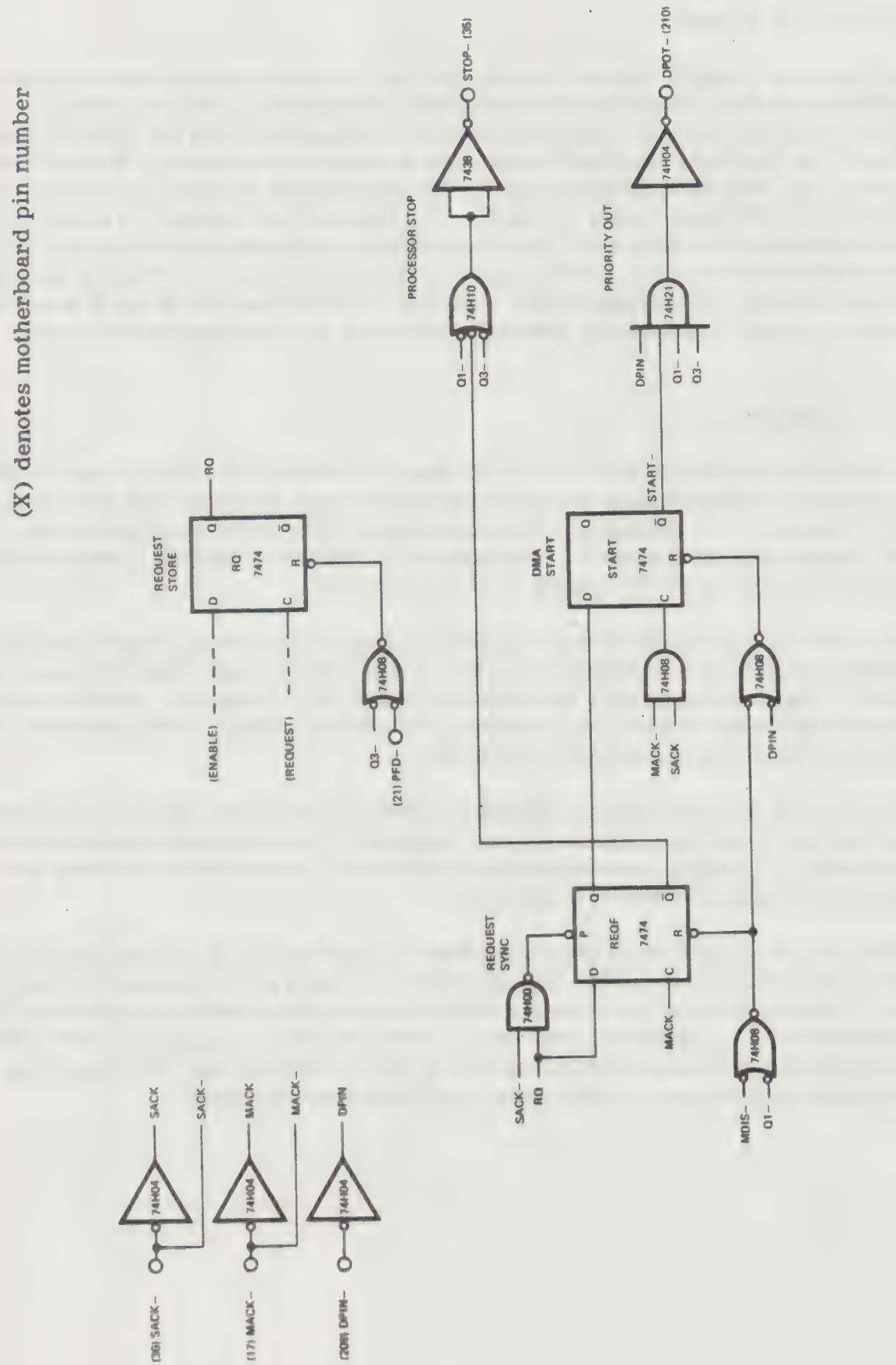


Figure 6-6. Maxi-Bus Acquisition and Priority Auction Controls

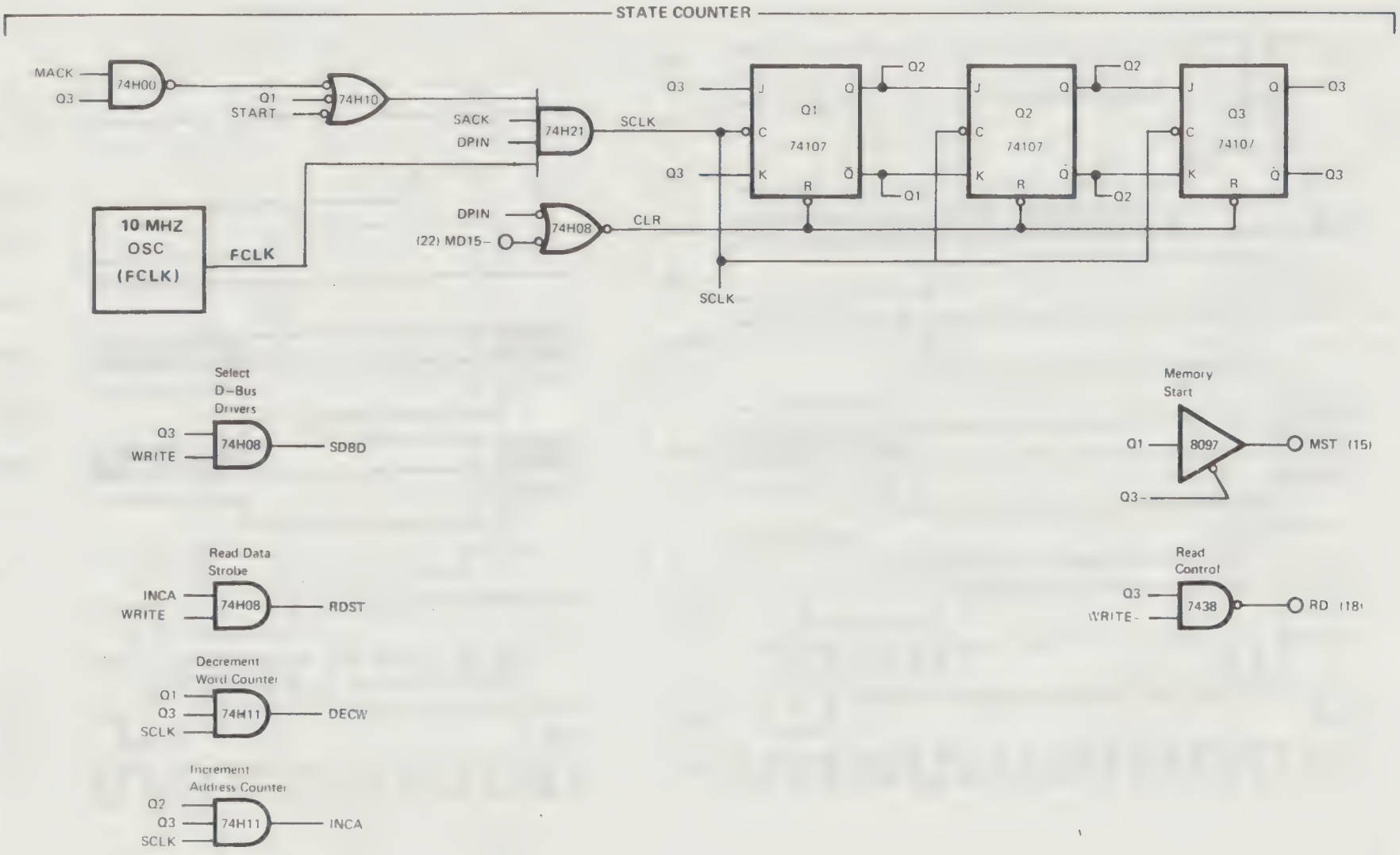
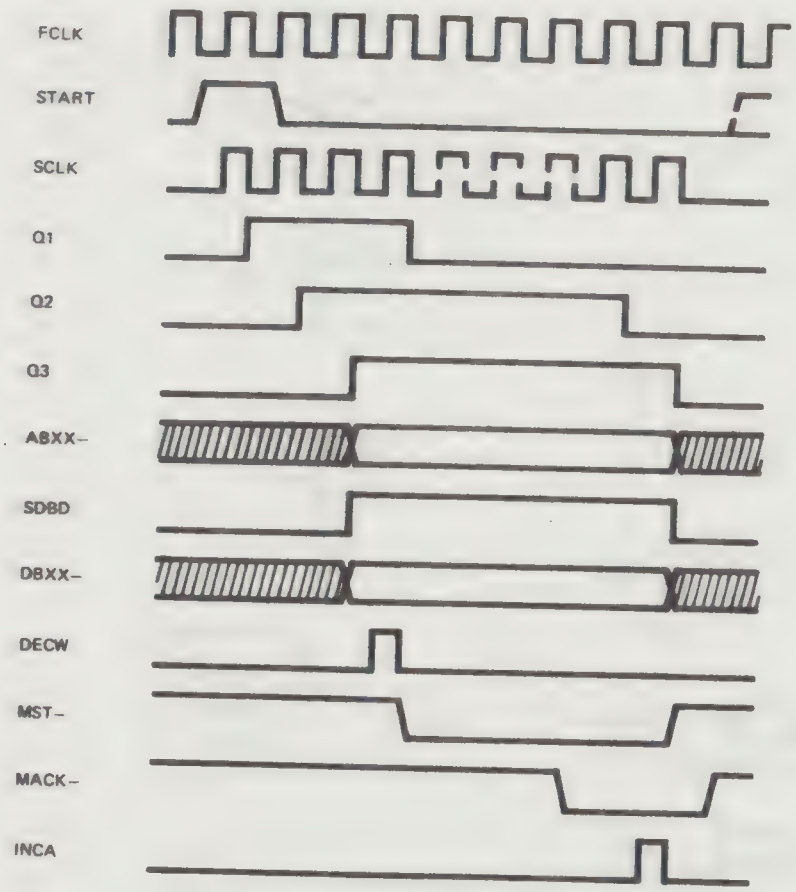
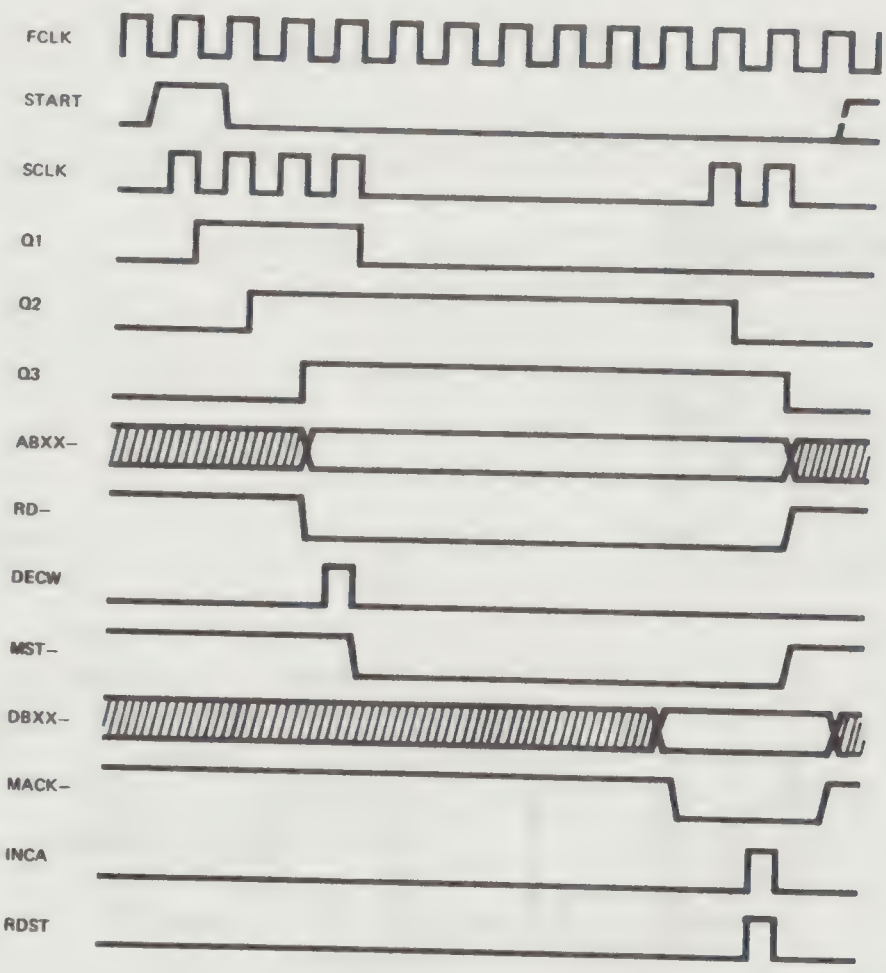


Figure 6-7. State Counter and Decoder



A. Write Cycle



B. Read Cycle

Figure 6-8. DMA Transfer Timing

COMPUTER AUTOMATION, INC.

6.4 BASIC DMA CONTROLLER ARCHITECTURE

A typical DMA controller interface between memory and a high speed peripheral device. It must be able to emulate the Processor in terms of controlling memory and making block data transfers of any length. A typical DMA controller must be able to perform the following operations:

1. Provide initialization sequencing by programmed I/O or DMA transfer.
2. Stop the Processor to sieze control of the Maxi-Bus.
3. Initiate a memory cycle.
4. Define either a read or write operation.
5. Provide temporary data storage and asynchronous data transfer to/from the associated peripheral.
6. Maintain the memory address for the current transfer and increment the address for the next transfer.
7. Maintain a count of the number of remaining transfers.
8. Provide error detection.
9. Terminate transfer operations (surrender Maxi-Bus to Processor) after the last transfer or upon an error indication.
10. Provide end of operation interrupt or status response.

A basic DMA controller features a control section, a word/byte counter, an address register/counter and a data channel as shown in Figure 6-9.

6.4.1 Control Section

The control section consists of initialization logic, a mode control register, Maxi-Bus acquisition controls, DMA priority logic and a 3-bit state counter and decoder.

The initialization logic is used to set up the DMA controller for subsquent operation. The initialization logic generates load signals for the mode control flags, the word counter and the address register. Two techniques can be used to implement the initialization logic. One technique involves the use of programmed I/O to set flags and load registers. An alternate technique involves the use of a sequencer and the DMA control logic to access a task control block in memory.

The Maxi-Bus acquisition controls issue the Processor STOP- signal in response to a DMA request.

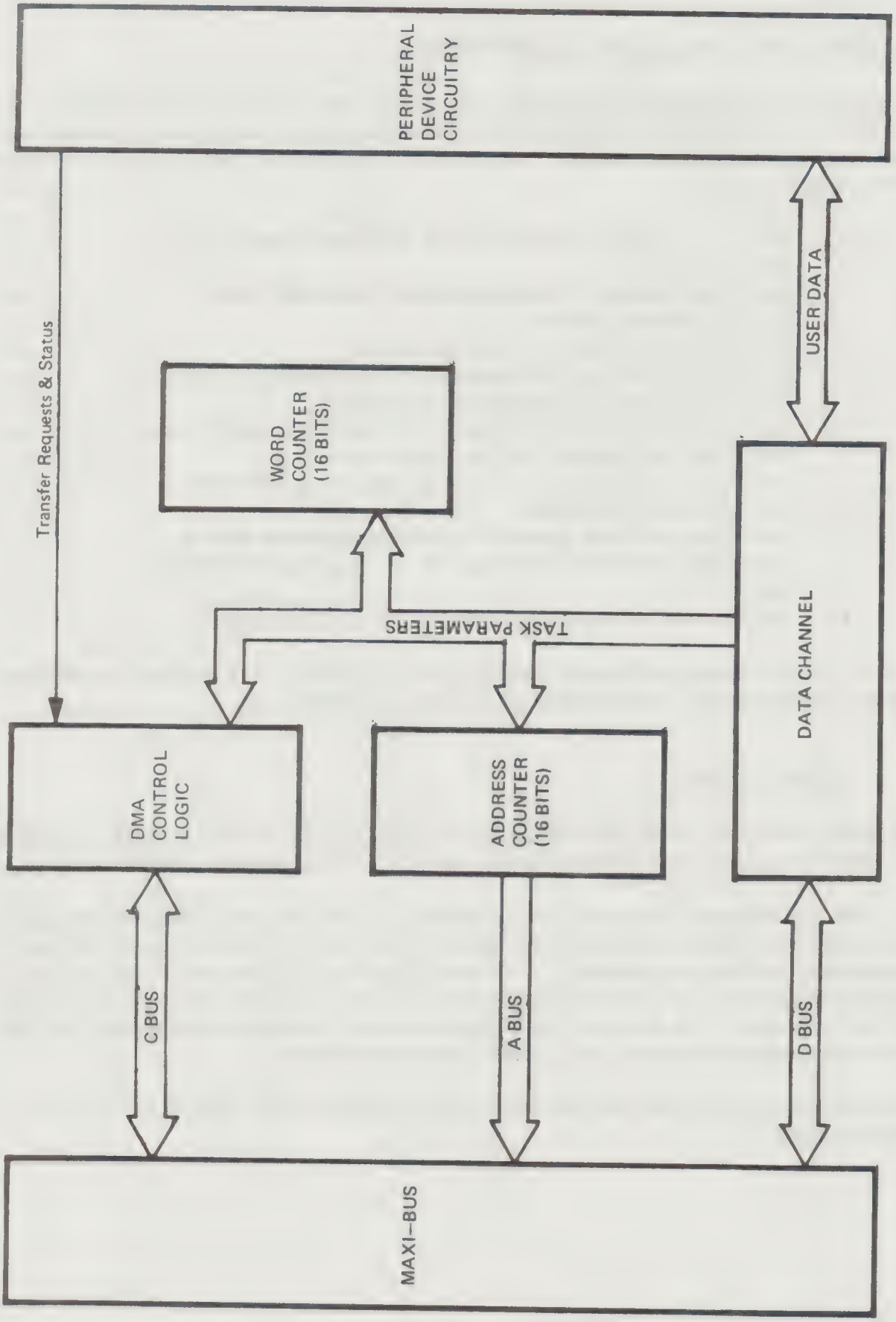


Figure 6-9. Basic DMA Controller Architecture

The DMA priority logic permits DMA operations between multiple DMA controllers. During each DMA cycle, the DMA priority is auctioned so that a higher priority DMA controller can transfer data.

The 3-bit state counter is used to time all operations during a data transfer. The decoder network decodes specific states of the state counter to generate a memory start signal, increment or decrement registers and gate data and address information to memory.

The mode control register has a minimum of 1-bit storage for the Read/write mode flag. If the user wishes to implement the Byte mode, a Byte mode flag is required to distinguish word transfers from byte transfers. The mode control register may be expanded to accommodate other user defined flags as deemed necessary.

6.4.2 Word/Byte Counter

The Word/Byte counter is a 16-bit parallel-loaded binary counter. During initialization, the word/byte count that corresponds to the total number of words or bytes to be transferred is parallel loaded into the register. During execution, the word/byte counter is decremented with each DMA transfer to or from memory. The word/byte counter also requires a word count equal-to-zero detection feature. This feature monitors the count during each transfer such that when the word count reaches zero, subsequent DMA requests are inhibited and termination operations are performed (typically an end-of-operation interrupt).

6.4.3 Address Counter

The address counter is a 16-bit parallel-loaded binary counter. During initialization, the starting address of the memory area being accessed is parallel loaded into the low order 15 bits of the counter. The MSB of the counter is set false for word mode and true for Byte mode. During execution, the address counter is incremented for each transfer (after MACK- is received). During Byte mode operations, the SLB flag (Select Least Significant Byte) is used as the LSB of the address count. When SLB- is low, the least significant byte of the transferred data word is read from or written into memory. Likewise, when SLB- is high, the most significant byte of the transferred data word is used. SLB- must be high (or not used) during word mode operation.

6.4.4 Data Channel

The data channel is a temporary storage element that serves as a staging area for DMA data transfers to or from memory. The complexity of the data channel is determined by two factors. The first factor is DMA latency. DMA latency is defined as the time required, under worst case conditions, for the Processor to surrender the Maxi-Bus

to a DMA controller. This worst case time for the NAKED MINI/LSI with the standard 1600 nanosecond memory is 5.6 microseconds (this is the maximum time that the Processor requires to do internal housekeeping and generate a Stop Acknowledge - SACK). The second factor that determines data channel complexity is the user's maximum data transfer rate when writing into memory.

Using the 5.6 microsecond DMA latency as a constant, the number of buffers that would be required for temporary data storage in the data channel is directly related to how many word transfers could be attempted prior to gaining control over memory. For instance, if the user has a data transfer rate of 750 kilowords per second, 1.3 microseconds would be required for each data transfer. With a latency of 5.6 microseconds and a transfer rate of 1.3 microseconds, a minimum of four words would be transferred and the transfer of a fifth word would have started before memory was under control. Thus, five buffers would be required for a 750 kiloword transfer rate. Furthermore, the memory capability would have to operate in the interleaved mode. The number of buffers required for various transfer rates are summarized in the following chart:

Data Transfers Up To	Number of Buffers Required
178,571 words/bytes/sec	1
357,142 words/bytes/sec	2
535,713 words/bytes/sec	3
714,284 words/bytes/sec interleaved	4
892,855 words/bytes/sec interleaved	5
1,071,426 words/bytes/sec interleaved	6
1,249,997 words/bytes/sec interleaved	7

The user can avoid the necessity of multiple buffers by use of a Hog Mode flip-flop. This flip-flop keeps the STOP-line active and disables downstream priority even though transfer requests are not occurring at a sufficient rate to sustain burst mode. In the burst mode, every memory cycle is dedicated to DMA transfers, i.e., 16-bit word transfer rate of 625 kHz (single memory). The TYP1- signal on the motherboard permits the DMA controller to sense which Processor is installed and perform Hog Mode transfers if necessary. TYP1- is ground when the Type 1 Processor is installed and is open when the Type 2 Processor is installed.

Section 7

INTERFACE CONTROLLER MECHANICAL CONSIDERATIONS

7.1 INTRODUCTION

This section discusses the mechanical design of a printed circuit board which can be installed in an ALPHA 16 LSI computer chassis.

Either full or half printed circuit boards may be used. When half boards are used, two half boards are joined together to form a full board.

All boards use bus bars to distribute power and ground to circuits. The bus bars minimize the ground and power etch runs, leaving more space on the board for signal etched circuit routing. The bus bar design permits etched circuitry to be routed underneath the bus bar with no danger of shorting.

Fiberglass stiffeners are used on all boards to eliminate sag and provide improved structural integrity.

7.2 CHASSIS CONSTRAINTS

The computer chassis is designed to accommodate a printed circuit board which has a width of 15 inches. All printed circuit boards are installed in the horizontal position. When installed, the chassis provides four-way support for the printed circuit board. The card guides support both sides of the printed circuit, the motherboard connectors support the front, and a notched card retainer supports the rear edge.

The thickness of the printed circuit board is determined by the motherboard connectors. A typical board is .062 inches thick. The motherboard connector permits variations in thickness ranging from .054 to .071 inches.

All components, stiffeners, bus bars, etc. are mounted on one side of the board. This side of a board is referred to as the "component side" while the other side is referred to as the "solder side". Boards are always installed with the component side up.

The chassis card guides are spaced on .75 inch centers. The height of components on the component side of a board and the lead protrusion on the solder side of a board must be minimized to permit unimpeded airflow and easier insertion and removal of printed circuit boards. All components should be no higher than .47 inch maximum. Lead protrusion should be held to .062 inch. maximum.

The card guides are an integral part of the computer chassis which is metal. To prevent short circuits on a board, the user should not permit any etched circuit runs that are closer than .200 inch from either edge of a board.

7.3 PRINTED CIRCUIT BOARD CONSIDERATIONS (Figures 7-1 thru 7.3)

Figures 7-1 and 7-2 show the critical dimensions, hole patterns for bus bars and stiffeners and the integrated circuit layout organization for a full and a half board, respectively.

The motherboard interface dimensions are extremely critical and must be adhered to rigorously.

The rear edge of the full board has room for two interface connectors. The 1.250 inch dimension from each edge is the area reserved for the card extractors (Part No. 40-06100-00). The .800 inch dimension at the center is the area reserved for the card retainer. The remaining area along the rear edge is connector area. The 6.350 inch dimension is the maximum allowable area that the mating connector can occupy. The overall length of a connector cannot exceed this dimension.

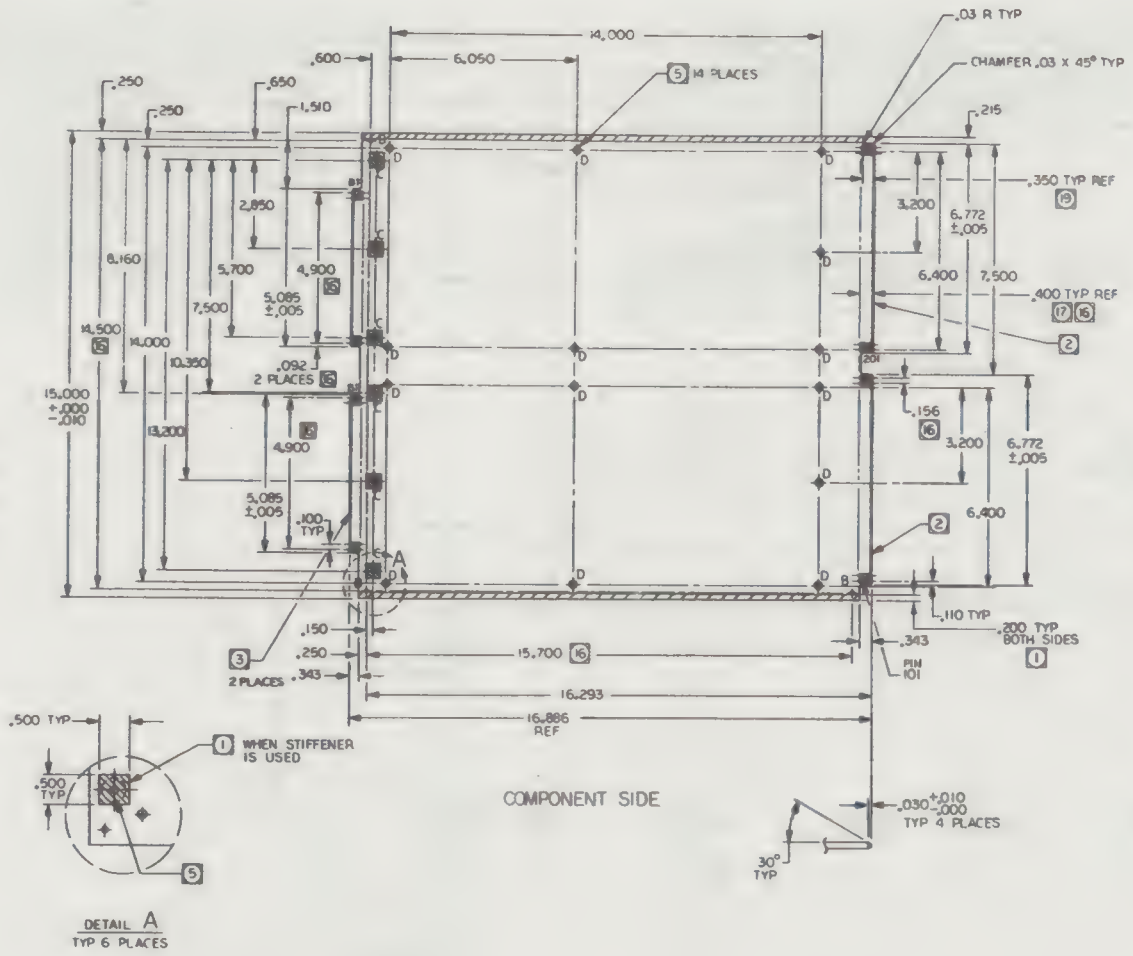
The rear edge of a half board has room for only one interface connector. A distance of 1.210 inch must be reserved for a modified card extractor (Part No. 00-00296-00). This leaves 5.080 inches of useable connector area remaining. The 5.080 dimension is the inside contact dimension of the standard 100-pin interface connector.

Half boards must provide for a card extractor at both rear corners although only one is installed depending upon which way the board is strapped to a second half card.

Figure 7-3 shows the standard printed circuit board hardware. All dimensions are provided for layout planning purposes. Connector data on the motherboard connector and various rear-edge interface connectors is also provided.

7.4 WIRE-WRAP BREADBOARD CARD

A half board wire-wrap breadboard card (Part Number 13234-00) is available from Computer Automation, Inc. This card features 72 IC sockets with wire-wrap posts, ground and power busses, and filters. This card can be useful for prototype development and checkout prior to making a formal printed circuit board design.



HOLE CHART					
NO.	FINISHED DIMENSION	REMARKS 20	QTY	SYMBOL	USAGE
A	.035 +.004 -.001	ON GRID PLATED THRU	A/R	REF	FOR IC'S AND ASSY COMPONENT LEAD UNDER .028 DIA MAX.
B	.089/.093	NO PLATING	3		TOOLING HOLES PART OF STD BOARD CONFIGURATION.
C	.140 +.004 -.001	NO PLATING	6		STIFFENER HOLES PART OF STD BOARD CONFIGURATION.
D	.140 +.004 -.001	NO PLATING	14		PIGGY BACK CARD & CONNECTOR MTG HOLES NON-STD.

24 PLATED THRU HOLES SHALL BE KEPT TO A MINIMUM OF DIFFERENT SIZES.

19 THIS AREA TO BE FREE OF SOLDER BOTH SIDES.

18. SHEETS AS SPECIFIED BELOW (SH. 1 THRU 7) COMPRISE A COMPLETE SET OF DOCUMENTS FOR FABRICATION OF A PCB.
    - SHEET 2 PAD MASTER.
    - 3 COMPONENT SIDE A/W.
    - 4 SOLDER SIDE A/W.
    - 5 COMPONENT SIDE SILKSCREEN MASTER.
    - 6 SOLDER SIDE SOLDER MASK.
    - SHEET 7 GROUND PLANE (IF REQUIRED).

17 CONTACT FINGER PLATING AREA.

16 THESE DIMENSIONS ARE DELINEATED ON ARTWORK. DIMS. ARE FOR REF. ONLY.

15. STAMP REVISION NO., COLOR BLACK, CHARACTER HEIGHT .090 MINIMUM.

14. SILKSCREENING TO BE YELLOW, COMPONENT SIDE PER SHEET 5, OR AS SPECIFIED.

13. ALL PLATED THRU HOLES TO CONFORM WITH 85-20017-00, SEC. 3.5.5.
    - (C) SOLDER PLATE REMAINDER OF BOARD PER 85-20017-00, SEC. 3.6.2 -5.
    - (B) SOLDER MASK SOLDER SIDE OF BOARD PER 85-20017-00, SEC. 3.8 (DARK GREEN).

12. FINISH: (A) FINGERS TO BE GOLD OVER NICKEL PER 85-20017-00, SEC. 3.6.1.3 AND 3.6.1.4.

11. MATERIAL: .063 THICK COPPER-CLAD, 2 SIDES, GLASS EPOXY. LAMINATE GF (FR4), 2 OZ AFTER PLATING.

10. FABRICATE PER THIS DRAWING AND C.A.I. SPECIFICATION 85-20017-00.

9. NOTES 10 THRU 19 ARE FABRICATION NOTES AND WOULD APPEAR ON SHEET 1 OF PWB FAB DETAIL DRAWING.

8. THE STANDARDS DEPICTED ON THIS DRAWING ARE SUBJECT TO CHANGE UPON WRITTEN APPROVAL FROM PROJECT ENGINEER.

7. FOR ASSEMBLY CONFIGURATION SEE LAYOUT 69-20079-00.

6. AREA UNDER STIFFENER (DWG'S 72-10048-00 & 72-20046-00) SHALL BE FREE OF COMPONENTS.

5 WHEN USING STANDARD #8 HARDWARE (.312 O.D. WASHER) ETCH FREE AREA SHALL BE: .400 DIA ON SOLDER SIDE, .250 DIA ON COMPONENT SIDE.
WHEN USING NON-STANDARD #4 HARDWARE (.250 O.D. WASHER) ETCH FREE AREA SHALL BE: .320 DIA ON SOLDER SIDE, .250 DIA ON COMPONENT SIDE & PROJECT ENGRN. SHALL BE CONSULTED.

4. ETCH SHALL BE NO CLOSER THAN .050 TO A EDGE (BOARD EDGE, CUTOUT, HOLE ETC.).

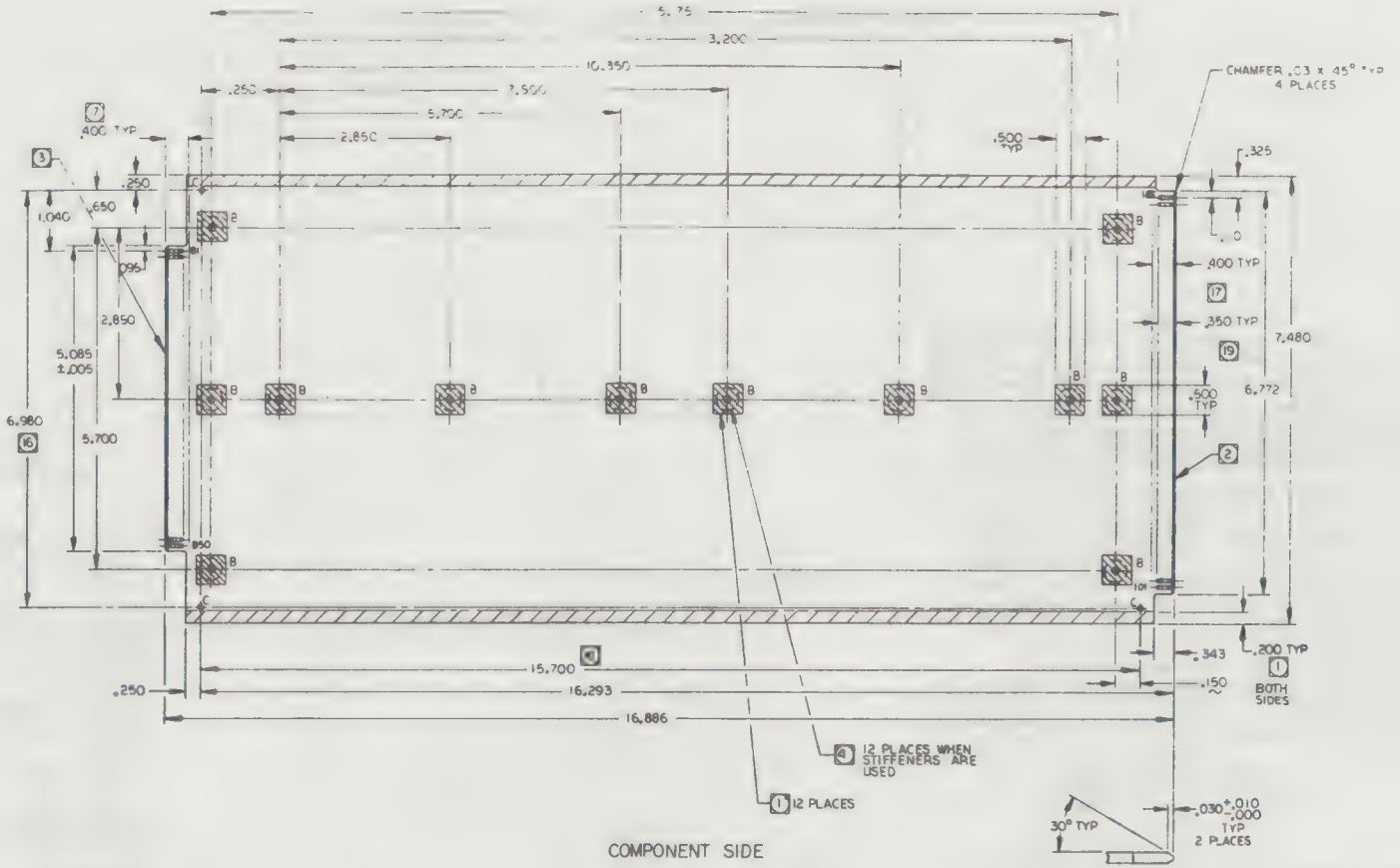
3 INTENDED TO MATE WITH CONNECTOR 17-10001-50 OR EQUIV.

2 INTENDED TO MATE WITH CONNECTOR 17-10035-01 / 17-10001-43 OR EQUIV.

1 SHADED AREA SHALL BE FREE OF FEED THRU HOLES AND ETCH.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 7-1. Full Board Design Guide



11. MATERIAL: .063 THICK COPPER-CLAD, 2 SIDES, GLASS EPOXY. LAMINATE GF(FR4), 2 OZ AFTER PLATING.
10. FABRICATE PER THIS DRAWING AND C.A.I. SPECIFICATION 85-20017-00.
9. NOTES 10 THRU 19 ARE FABRICATION NOTES AND WOULD APPEAR ON SHEET 1 OF PWB FAB DETAIL DRAWING.
8. ETCH SHALL BE NO CLOSER THAN .050 TO A EDGE OF A CUTOUT, HOLE, ETC.
7. FOR ASSEMBLY CONFIGURATION SEE LAYOUT 69-20079-00.
6. AREA UNDER STIFFENER (DWG'S 72-10048-00 & 72-20046-00) SHALL BE FREE OF COMPONENTS.
5. THE STANDARDS DEPICTED ON THIS DRAWING ARE SUBJECT TO CHANGE UPON WRITTEN APPROVAL FROM PROJECT ENGINEER.

[4] WHEN USING STANDARD #4 HARDWARE (.312 O.D. WASHER) ETCH FREE AREA SHALL BE: .400 DIA ON SOLDER SIDE.
WHEN USING NON STANDARD #4 HARDWARE (.250 O.D. WASHER) ETCH FREE AREA SHALL BE: .320 DIA ON SOLDER SIDE.
PROJECT ENGINEERING SHALL BE CONSULTED.

[3] INTENDED TO MATE WITH CONNECTOR 17-10001-50, OR EQUIV.

[2] INTENDED TO MATE WITH CONNECTOR 17-10035-01 / 17-10001-43, OR EQUIV.

[1] SHADED AREA SHALL BE FREE OF FEED THRU HOLES AND ETCH.

NOTES: UNLESS OTHERWISE SPECIFIED

[20] PLATED THRU HOLES SHALL BE KEPT TO A MINIMUM OF DIFFERENT SIZES.

[19] THIS AREA TO BE FREE OF SOLDER BOTH SIDES.

18. SHEETS AS SPECIFIED BELOW (SH 1 THRU 7), COMPRISE A COMPLETE SET OF DOCUMENTS FOR FABRICATION OF A PCB.
SHEET 2 PAD MASTER.
3 COMPONENT SIDE A/W.
4 SOLDER SIDE A/W.
5 COMPONENT SIDE SILKSCREEN MASTER.
6 SOLDER SIDE SOLDER MASK.
SHEET 7 GROUND PLANE (IF REQUIRED).

[17] CONTACT FINGER PLATING AREA.

[16] THESE DIMENSIONS ARE DELINEATED ON ARTWORK. DIMS. ARE FOR REF. ONLY.

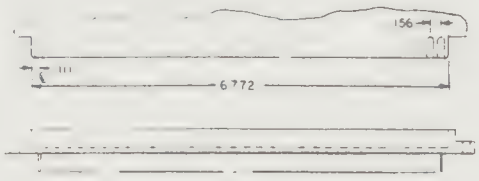
15. STAMP PART NO & REVISION LETTER, COLOR BLACK, CHARACTER HEIGHT .090 MINIMUM.
14. SILKSCREENING TO BE YELLOW, COMPONENT SIDE PER SHEET 5, OR AS SPECIFIED.
13. ALL PLATED THRU HOLES TO CONFORM WITH 85-20017-00, SEC. 3.5.5.
(C) SOLDER PLATE REMAINDER OF BOARD PER 85-20017-00, SEC. 3.6.2 & 5.
(S) SOLDER MASK SOLDER SIDE OF BOARD PER 85-20017-00, SEC. 3.8 (DARK GREEN).
12. FINISH: (A) FINGERS TO BE GOLD OVER NICKEL PER 85-20017-00, SEC. 3.6.1.3 & 3.6.1.A.

HOLE SCHEDULE

NO.	FINISHED DIMENSION	REMARKS [4]	QTY	SYMBOL	FUNCTION
A	.035 +.004 -.001	ON GRID PLATED THRU	A/R	REF	
B	.140 +.004 -.001	NO PLATING	12	◆	STIFFENER HOLES
C	.089/.093	NO PLATING	3	◆	TOOLING HOLES FOR HALF CARD

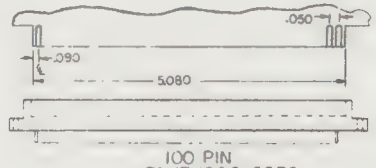
Figure 7-2. Half Board Design Guide

MOTHERBOARD CONNECTOR

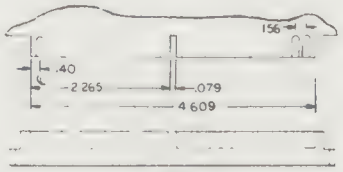


86 PIN
PN 17-10001-43P0

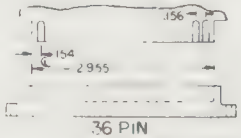
REAR EDGE CONNECTOR VARIATIONS



100 PIN
PN 17-10001-50P0



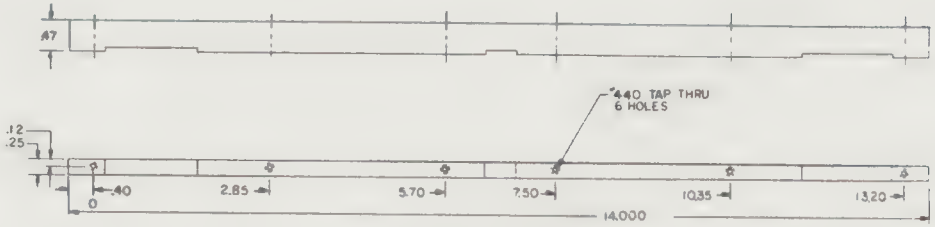
56 PIN
PN 17 10002 28P1



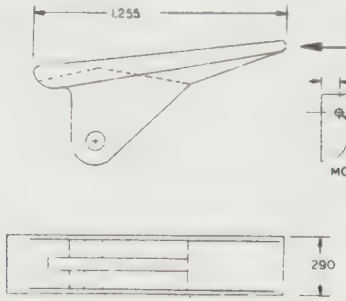
36 PIN
PN 17-10002-18P1

BUS BAR (PN00-00285-00)

STIFFENER (PN00-00160-00)



FULL BOARD CARD EXTRACTOR (PN40-06100-00N0)



NOTE: The half-board card extractor (PN00-00296-00) is the same as the full-board extractor, except .130 inches of material are removed from the tip of the extractor.

Figure 7-3. Standard Circuit Board Hardware

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Section 8

INTEGRATION

8.1 INTRODUCTION

This section provides detailed information pertaining to the mounting, cooling, and interconnection of either the ALPHA LSI or NAKED MINI LSI Type 1 and Type 2 computers.

8.2 ALPHA LSI INTEGRATION

The following paragraphs discuss mounting, cooling, installation of cards, and AC power application for the ALPHA LSI computer.

8.2.1 Mounting (Figure 8-1)

The ALPHA LSI computer is designed to be panel mounted in a standard 19-inch rack or cabinet. Figure 8-1 provides outline and mounting dimensions to facilitate installation of the computer.

8.2.2 Cooling (Figure 8-2)

The ALPHA LSI Computer is designed to operate over a temperature range of 0° C to 50° C. When the computer is installed in an enclosure, the installation requirements depend on the ventilating system employed such that the thermal requirements of the computer are maintained.

There are three installation criteria which provide the minimum cooling conditions allowable for the ALPHA LSI computer.

1. Closed Ventilation System
2. Side Ventilation System
3. Top/Bottom Ventilation System

In the closed ventilating system it is assumed the ambient temperature will be maintained by the thermal interface. The minimum size enclosure must provide adequate air flow paths for the computer internal fans.

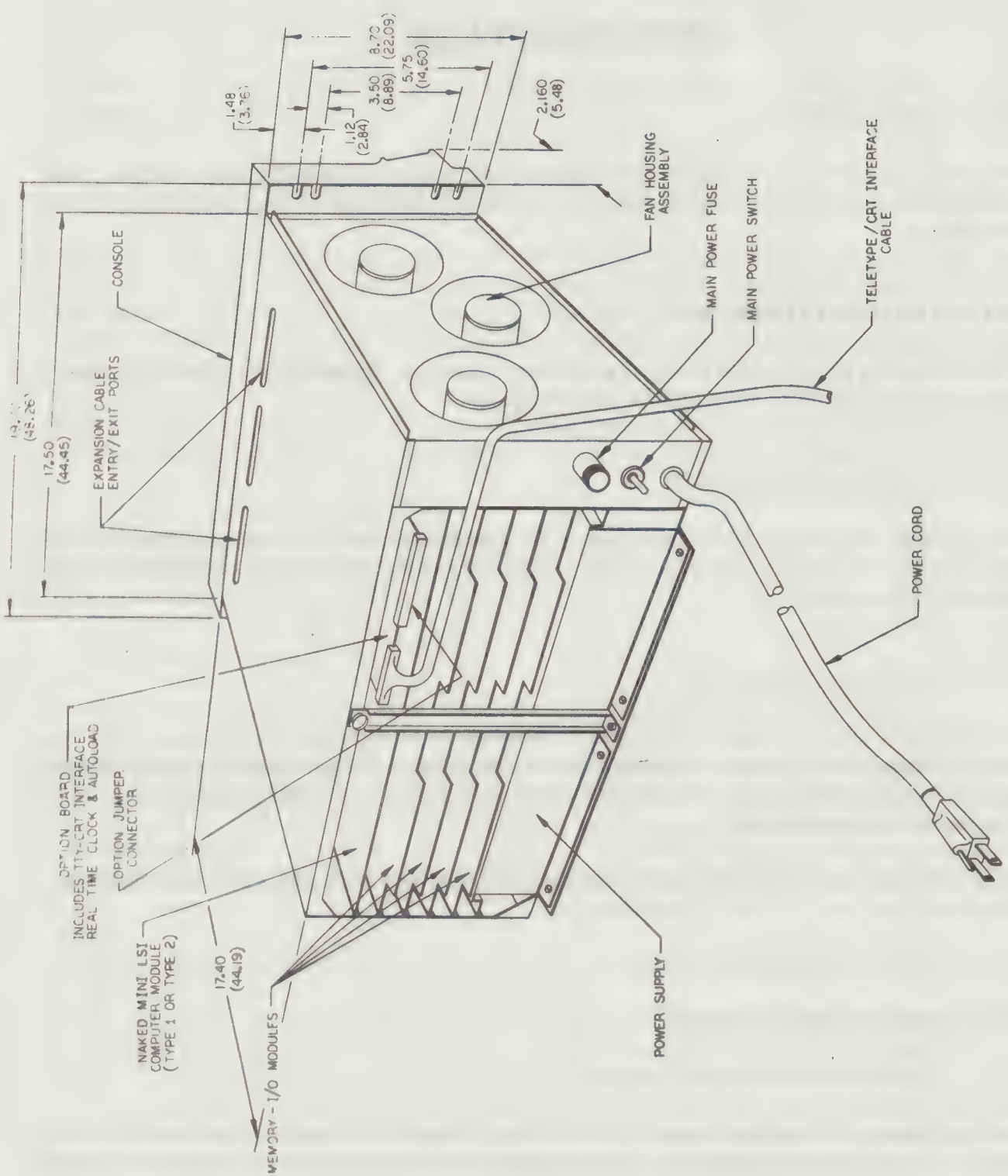
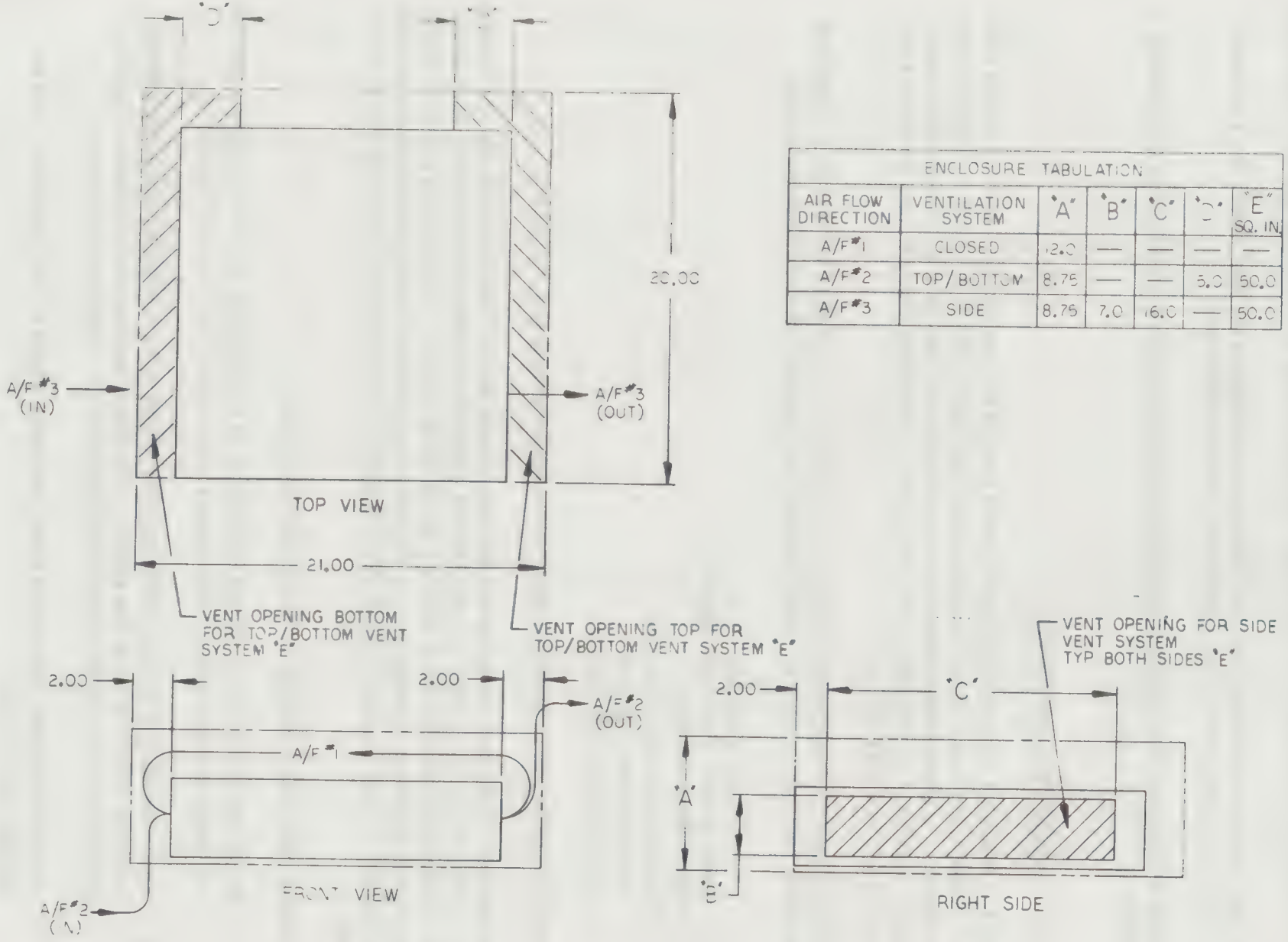


Figure 8-1. ALPHA LSI Outline and Mounting



ENCLOSURE TABULATION						
AIR FLOW DIRECTION	VENTILATION SYSTEM	"A"	"B"	"C"	"D"	"E" SQ. IN.
A/F #1	CLOSED	12.0	—	—	—	—
A/F #2	TOP/BOTTOM	8.75	—	—	5.0	50.0
A/F #3	SIDE	8.75	7.0	16.0	—	50.0

Figure 8-2 ALPHA LSI Ventilation Systems

The side ventilating system establishes the minimum enclosure size and rectangular surface for the minimum size opening. This provides for a safety guard if necessary.

The top/bottom ventilating system defines the minimum airflow paths for a cabinet with stacked equipment or an individual console enclosure.

Figure 8-2 defines the minimal dimension parameters for each of these ventilating systems.

8.2.3 Joining Two Half Cards

Most I/O modules occuply only half a card slot in the computer. When several half card options are used, it is recommended that half cards are joined together to form full cards. In those cases where an odd multiple of half card I/O modules is used, a blank half card is available from Computer Automation, Inc. to join with the last card (Part No. 13234-00).

Half card modules are joined together by means of a stiffener kit which is supplied with each half card module. Each stiffener kit consists of the following parts:

1. Two 14-inch stiffener bars
2. Eight 4-40 x .500 inch screws
3. Eight fiber washers
4. One nylon card extractor
5. One extractor roll pin
6. One interface connector

When joining two half cards together, two stiffener kits are required.

The stiffener bars are installed on the component side of each printed circuit board. One stiffener bar is located parallel to the computer interface contacts on each module. Another stiffener bar is located at the back edge of each module parallel to the peripheral interface contact strip. Finally, two stiffener bars (one for each module) are located on the adjacent edges of each module (what would be the center of a full card).

Stiffener bars are installed in the following manner:

1. First determine the physical placement of the module in the computer, that is, the relative placement of the module with regard to the priority string.

2. Next, install the center stiffener bars. The nylon screw is inserted through from the solder side of the board. The fiber washer goes between the component side of the board and the stiffener bar. Tighten the screws.

3. Install a stiffener bar on the front and rear edges of both modules. Do not tighten the screws.

4. Next, find a level work surface. Stand both modules in a vertical position with the front edge down. Ensure that the contact edge of each module is touching the table surface and that the modules are butted together. Tighten the nylon screws on the front edge. Now tighten the screws on the back edge.

5. Finally, examine the card extractors on one of the Processor boards in the computer. Find the similar extractor mounting holes on each module. Mount the extractor on each side of the module and insert the roll pin.

This completes the joining operation. The card is now ready to install in the computer. When all cards are installed, be sure to install the card retainer at the rear of the computer.

8.2.4 Option Card Installtion

The option card mounts in piggyback fashion to the left half (as viewed from the front) of either the LSI-1 or LSI-2 Processor module. Support standoffs are provided with the Processor modules. All loose hardware (screws, lockwashers, washers and rear-edge connectors) is provided with the option card.

The option card has three edge connectors. Connector P1 interfaces with J1 on the Processor Module. Connector J1 is the option jumper connector and connector J2 is the Teletype interface connector. Detailed information about the use of connectors J1 and J2 is provided in Section 11 of this manual.

To install the option card, proceed as follows:

1. Take the option card and insert J1 and J2 thru the slots in the rear stiffener of the Processor module.

2. Position connector P1 for insertion into connector J1 on the Processor module.

3. Gently push the option card into Processor connector J1 aligning the four mounting holes with the Processor module standoffs.

4. Install a screw, lockwasher, and washer in each standoff and tighten.

5. Install rear edge connectors per instructions in Section 11.

8.2.5 Module Installation

CAUTION

Do not remove or install any PC cards while power is applied to the computer.

The ALPHA LSI motherboard slot organization is shown in Figure 2-2. The following rules apply to the placement of processor modules, memory modules and interface modules.

1. Install all modules with component side up.

2. Install the NAKED MINI LSI Computer Module (either Type 1 or Type 2) in the top slot (slot A).

3. Install memory modules next.

4. Install DMA controller(s) after memories.

5. Install I/O modules. I/O priorities are determined by physical location of the interface modules within the Chassis. I/O priorities begin with slot B200 and weave through the motherboard as shown in Figure 4-2. The priority line is routed through each interface so that is can inhibit the lower priority devices when requesting service. Therefore, all I/O modules must be placed in consecutive priority level slots immediately following the memory modules to provide continuity in the priority chain. If the priority chain is broken, down-stream interrupts may not be serviced. If they are serviced, they will be serviced improperly.

6. Install the card retainer and install rear edge cables.

An Interface Description document is supplied with each I/O interface module. This document defines the software and cabling requirements of the interface module. Refer to the Interface Description to resolve any questions about the interface module.

CAUTION

All I/O interface modules must have the rear-edge cable connector installed prior to operation of the Processor. If the connector is not installed, a default device address of zero will be assigned to the module, causing improper instruction execution. Device address zero is reserved exclusively for Processor use. For details concerning assignment of a unique device address to each I/O interface module, refer to the associated interface description which is packed with each module.

8.2.6 AC Power Application

Before plugging the AC line cord into a power source, be sure that the main power switch, located on the back of the chassis, is in the OFF position. Plug the AC line cord into the power source.

CAUTION

Connect AC line cord to properly grounded 3-prong outlet only.

NOTE

When AC power is applied, the fans will operate when the main power switch is in the ON position. Ensure that they are operating.

8.2.7 110/220 Power Line Conversion

The ALPHA LSI computer may be powered from either 110 Vac or 220 Vac. To convert from 110 Vac to 220 Vac, or vice-versa, proceed as follows:

1. Turn off power and remove line cord from AC power source.
2. Remove console from front of chassis.
3. Disconnect power pigtail connector from the power supply.

All conversions are made at the pigtail connector as follows:

From 110 to 220	From 220 to 110
Remove jumper from P1-1 to P1-3	Remove jumper from P1-2 to P1-3
Remove jumper from P1-2 to P1-4	Move wire from P1-4 to P1-2
Move wire from P1-2 to P1-4	Add jumper from P1-1 to P1-3
Add jumper from P1-2 to P1-3	Add jumper from P1-2 to P1-4

4. Install power pigtail in power supply.
5. Install console.
6. Install line cord, turn on power and checkout unit.

8.3 NAKED MINI LSI INTEGRATION

The following paragraphs discuss mounting, cooling and interconnection of the NAKED MINI LSI Type 1 and Type 2 computers.

8.3.1 Mounting

There are two mounting considerations. One for LSI-1 and one for LSI-2.

8.3.1.1 LSI-1 Mounting (Figure 8-3)

The LSI-1 computer may be mounted in any plane as long as the cooling requirements are satisfied. The computer may be hard mounted with mobile or fixed interface connector or slide mounted with fixed interface connectors.

Five mounting holes are provided for hard mounting. Two holes are at the front of the module near the corners, two are at the back of the module and one hole is located in the center of the module. It is recommended that standoffs be used when hard mounting the computer.

For slide mounting, a clear area of 0.200 inches is provided along each side of the module to accommodate various types of card guides. The card guide should be able to handle a printed circuit board thickness of 0.062 inches. The LSI-1 computer module should be supported along all four edges. The interface connectors along the front of the module should be hard mounted to the users structure and some type of support should be provided at the rear of the module.

8.3.1.2 LSI-2 Mounting

The LSI-2 is mounted in the same manner as the ALPHA LSI. Refer to paragraph 8.2.1 and Figure 8-1.

8.3.2 Cooling

The cooling requirements for the LSI-1 and LSI-2 are discussed below.

8.3.2.1 LSI-1 Cooling

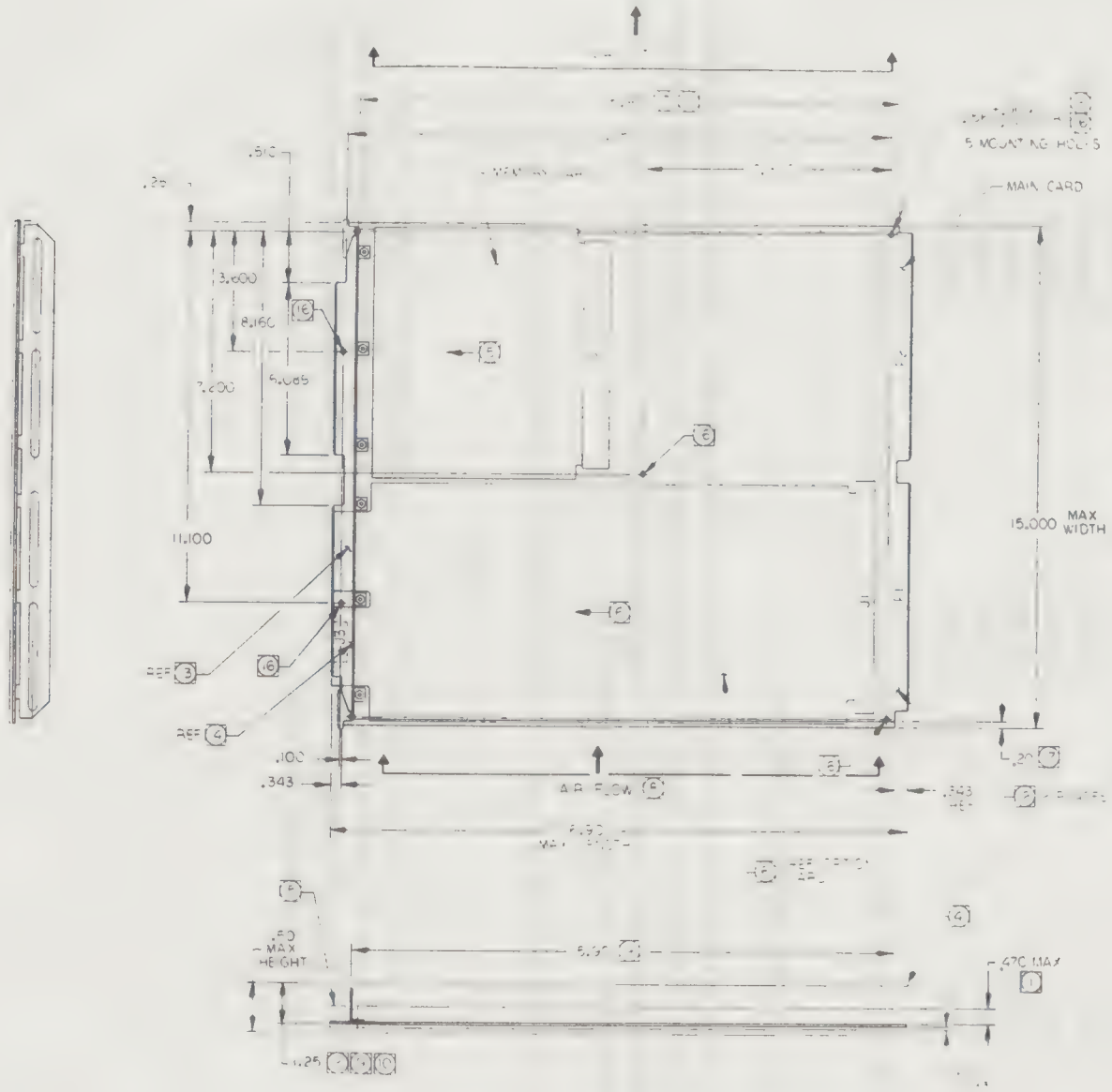
The LSI-1 computer is designed to operate over a temperature range of 0° C to 50° C. Cooling air must flow from the Processor side of the module to the memory side of the module. Notes 8, 9, and 10 of Figure 8-3 must be adhered to.

8.3.2.2 LSI-2 Cooling

The LSI-2 chassis has a fan housing with three fans. These fans provide adequate cooling for the computer.

8.3.3 Interconnection

The interconnection requirements of the LSI-1 and LSI-2 are discussed below.



NOTES: UNLESS OTHERWISE SPECIFIED

1. MAXIMUM COMPONENT HEIGHT OF MAIN CARD.
2. MAXIMUM HEIGHT OF MEMORY CARD & OPTION CARD (OPTION CARD NOT SHOWN).
3. CLEAR AREA (ETCH OR FEED THRUS) .350 DIA MINIMUM AROUND MOUNTING HOLES BOTH SIDES.
4. THE MEMORY AND OPTION CARD ARE ACCESSABLE FROM THE SURFACE INDICATED.
5. THE MEMORY CARD IS ACCESSABLE BY THE REMOVAL OF TWO (2) #4 SCREWS AND PULLING THE CARD FROM THE CONNECTOR IN THE DIRECTION SHOWN.
6. THE OPTION CARD IS ACCESSABLE BY THE REMOVAL OF FOUR (4) #4 SCREWS AND PULLING THE CARD FROM THE CONNECTOR IN THE DIRECTION SHOWN.
7. THE NAKED MINI ALPHA LSI COMPUTER MAY BE MOUNTED IN ANY PLANE PROVIDING NOTES 8,9 & 10 ARE ADHERED TOO.
8. AIR FLOW SHALL BE IN THE INDICATED DIRECTION ONLY.
9. AIR SHALL BE SUPPLIED AT THE VOLUME OF 20 CFM MINIMUM WITH A MAXIMUM PRESSURE DROP OF .2 INCHES OF WATER THROUGH AN AIR CORRIDOR AS INDICATED.
10. OBSTRUCTIONS AND AIR LEAKS SHALL BE ALLOWABLE TO THE EXTENT THAT A MINIMUM OF 150 FPM OF AIR IS EXHAUSTED FROM ANY PART ACROSS THE OUTPUT SIDE OF THE COMPUTER MAIN CARD AS INDICATED.
11. THE NAKED MINI ALPHA LSI COMPUTER SHALL BE KEPT FREE OF EXCESSIVE FOREIGN MATERIAL (OIL, DUST, SALTS, ETC).
12. MATES WITH CONNECTOR (VIKING P/N 2VK43D/-12 OR EQUIVALENT.
13. MATES WITH CONNECTOR (WINCHESTER P/N 88CJ 85) OR EQUIVALENT.
14. MATES WITH CONNECTOR (VIKING P/N 2VH25/ JN-5) OR EQUIVALENT.
15. MATES WITH CONNECTOR (
16. [illegible] MOUNTING HOLES.
17. [illegible] BE [illegible] EACH SIDE OF THE MAIN CARD [illegible] MOUNTING HOLES TO PREVENT [illegible].

5 MOUNTING HOLES

Figure 8-3. LSI-1 With Core Memory Outline and Mounting

8.3.3.1 LSI-1 Interconnection

The LSI-1 interconnections consist of bringing power to the module, strapping the Maxi-Bus across from P1 to P2 and interfacing the system control console to P1.

There are ten special signals that interface with the P1 connector that are not part of the Maxi-Bus. Eight of these signals are dedicated console interface signals while the other two are dedicated power supply signals. Under no circumstances should these signals be strapped across to the P2 connector. These dedicated signals and their pin assignments are listed below.

Signal	Pin	Dedicated to
SSW-	P1-9	Console
IF-	P1-10	Console
TTLF-	P1-11	Power Supply
+5H	P1-12	Power Supply
AL-	P1-33	Console
BM-	P1-34	Console
OV-	P1-37	Console
START-	P1-38	Console
SERV-	P1-83	Console
CINT-	P1-84	Console

Table 2-1 lists Maxi-Bus and power signals and pin assignments.

8.3.3.2 LSI-2 Interconnections

All LSI-2 interconnections are made at the motherboard. Motherboard connector J1 provides the console interface while connector F100 provides the power interface. Console interface information is available in Section 9 while power supply interface information is available in Section 10.

To convert the LSI-2 from 110 Vac to 220 Vac, refer to paragraph 8.2.7.

NOTE

The user must provide a 220 to 110 Vac stepdown transformer to power the fans in the chassis. The fan wiring should be moved from P1-1 and P1-2 to the secondary of the transformer. The transformer must be capable of 0.6 amps fan load.

Section 9

CONSOLE INTERFACE REQUIREMENTS

9.1 INTRODUCTION

A console, be it the standard ALPHA/LSI console or a user designed console, is an I/O device with a special set of dedicated I/O instructions with special mnemonics.

The console is assigned device address 0 (DAO) and shares this device address with the Power Fail/Restart option, the Autoload option and the console interrupt and trap controls of the Processor.

The console communicates with the Processor via the Maxi-Bus and uses a special set of control signals (not considered part of the Maxi-Bus) to stop, step, and start the Processor.

This section provides a detailed discussion of interface signals, transfer timing, data formats, etc. This section also discusses the minimum requirements of a console and how to add features to the minimum console.

9.2 CONSOLE - PROCESSOR INTERFACE (Figure 9-1)

The Console interfaces to the Processor via the Maxi-Bus, plus special control lines not considered to be part of the Maxi-Bus. The special lines and the associated functions are described below:

SERV- Console Service. The SERV- signal (ground-true) is issued by the console to command the Processor to service the console. The SERV- line may be considered to be an interrupt line with priority over all interrupts, but superseded by DMA operations. The Processor responds to SERV- by performing a Console Control Word (CCW) input (actually, an instruction fetch from the console instead of memory). The CCW determines the required servicing.

IF- Instruction Fetch. The IF- signal (ground-true), issued by the Processor, envelops the instruction fetch cycle. In response to SERV-, the Processor performs an instruction fetch cycle, which in this case is a CCW fetch instead of the usual memory read cycle. The console uses IF- to differentiate the CCW input cycle from a status word input cycle; both use device address and function code zero.

If SERV- is issued coincident with the leading edge of IF- or later, the instruction fetch cycle will cause an instruction to be accessed from memory and subsequently executed before SERV- will be honored. SERV- must lead IF- by at least 1.6 microseconds to guarantee that the next IF- cycle will be a CCW input cycle.

START- Start Processor. Signal START- (ground true) is issued by the console to command the Processor to resume processing. START- must be a minimum of 1.6 microseconds wide. The Processor resumes processing on the trailing edge of START-. Signal SERV- must precede the trailing edge of START- by at least 1.6 microseconds to guarantee that the Processor will immediately perform a CCW input instead of a memory read cycle when processing is resumed.

CINT- Console Interrupt. CINT- (ground-true) is issued by the console to interrupt normal processing. Signal CINT-, once issued, must be held true until signal IAR- (Interrupt Acknowledge) is true.

SSW- Sense Switch. Signal SSW- (ground-true), issued by the console, tracks the console SENSE switch. No synchronization is required. If the SENSE switch is set, signal SSW- is true.

AL- Autoload. Signal AL- (ground-true) is issued by the console to command the optional autoload logic to perform an autoload sequence. The autoload sequence is initialized on the leading edge of AL- and commences on the trailing edge of AL-. The AL- pulse width must be 100 nanoseconds minimum.

OV- Overflow. The OV- signal (ground-true) is issued by the Processor. OV- tracks the Overflow flip-flop internal to the Processor.

BM- Byte Mode. The BM- signal (ground-true) is issued by the Processor. BM- tracks the Byte Mode flip-flop internal to the Processor.

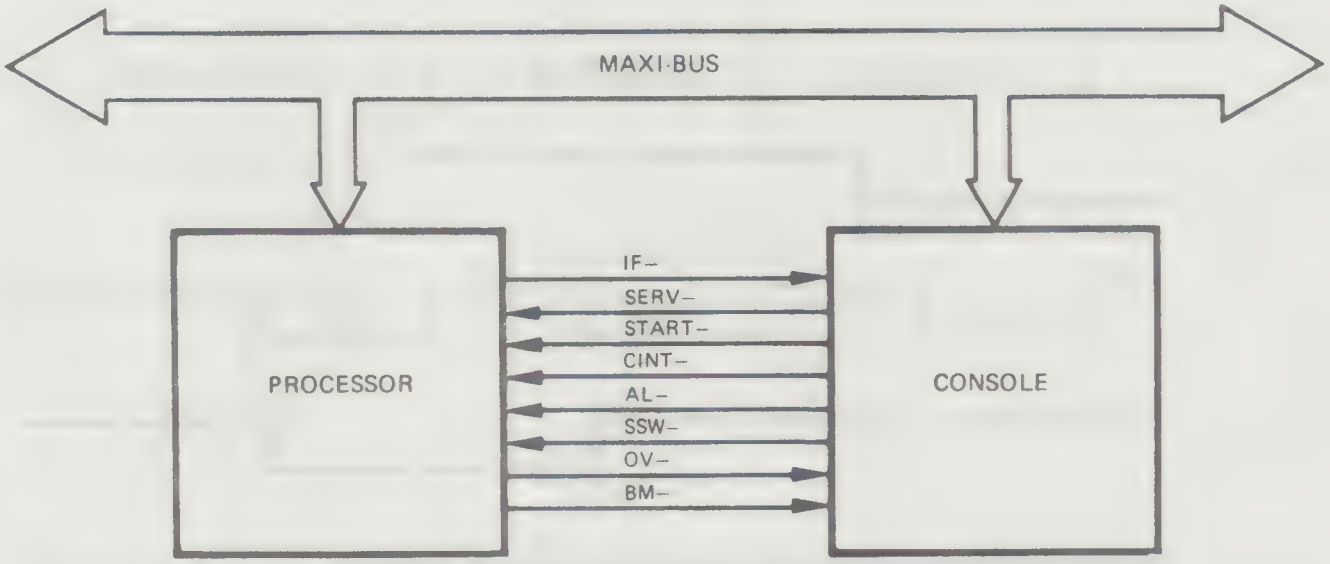


Figure 9-1. Processor/Console Interface

9.3 CONSOLE TRANSFER TIMING

There are four basic functions (beyond normal I/O functions) that a console can perform which are: establishment of the Stop Mode, register entry and display, Step-Mode operation, and establishment of the Run Mode. The timing requirements for each of these functions are discussed in the following paragraphs.

9.3.1 Establishment of Stop Mode (Figure 9-2)

During the Run Mode, the Processor Instruction Fetch signal (IF-) is ground-true when the Processor is fetching an instruction from memory and is high during the execution of the instruction. The console uses the trailing edge of the IF- signal to synchronize the generation of a Console Service Request (SERV-).

The Stop Mode is initiated by operator activation of the console STOP switch. With the STOP switch active, the SERV- signal is enabled. SERV- goes ground-true during the execution period of the current instruction and remains ground-true for the next instruction fetch.

Upon seeing the SERV- signal active, the Processor fetches the next instruction from the console rather than from memory. When the Processor fetches the instruction from the console, it addresses device address 0 and function code 0 and issues the IN- control signal. The console, upon seeing IF- low, device address and function code 0 and IN- low, places a Stop CCW word on the data bus.

The Processor vectors the STOP CCW word to its instruction register and executes the instruction. The CCW instruction algorithms causes the Processor to halt.

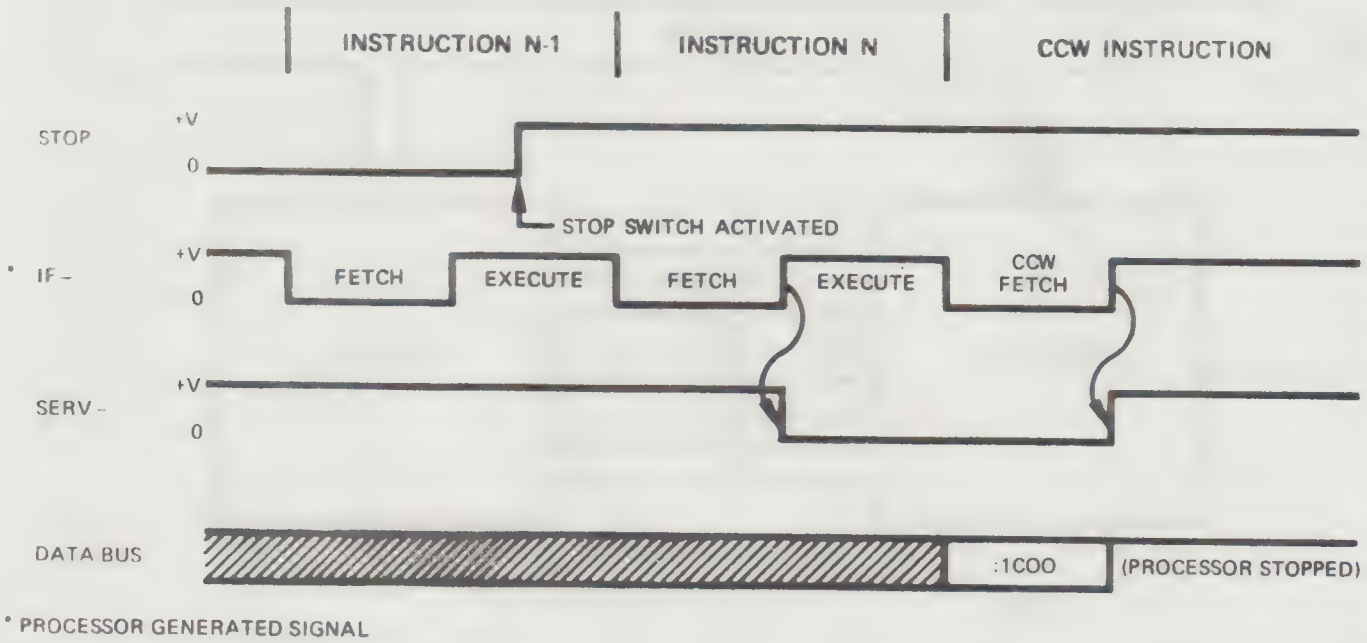
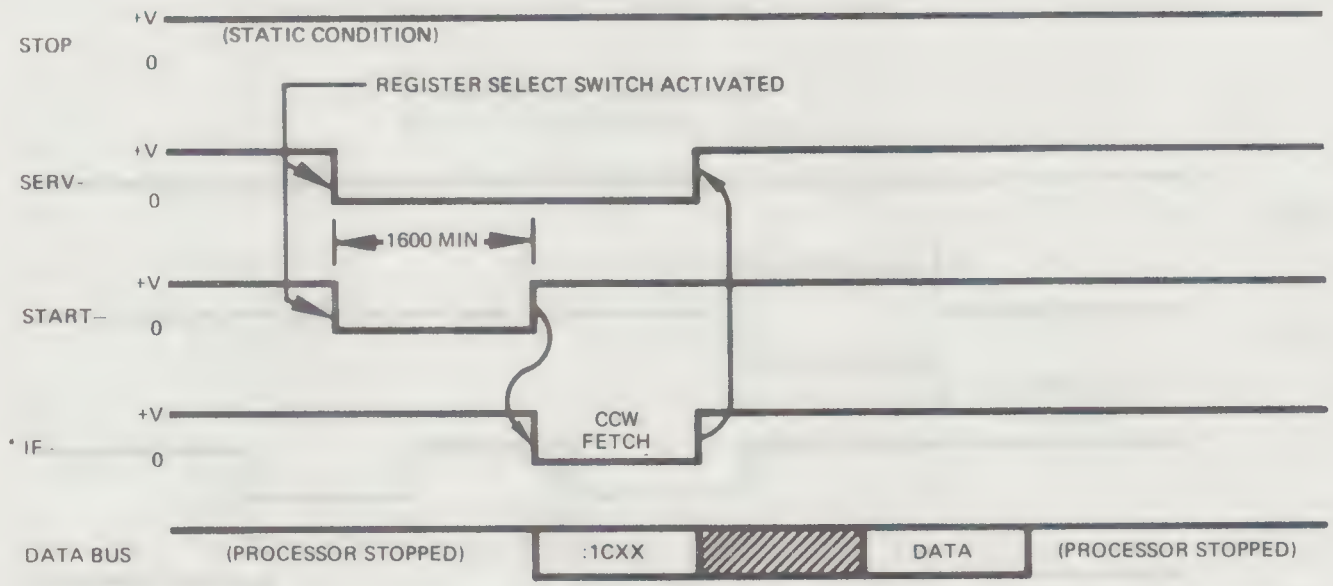


Figure 9-2. Establishment of Stop Mode.

9.3.2 Register Entry and Display (Figure 9-3)

The register entry and display sequence can be performed only when the Processor is stopped. The sequence is initiated by activation of a Register Select switch on the console. The switch activation causes both SERV- and START- (Processor Start) to go low, simultaneously. Approximately 1600 nanoseconds later, the Processor resumes operation on the trailing edge of START-.

Upon resumption of operation, the Processor recognizes that the SERV- signal is active and fetches the next instruction from the console. The console upon seeing IF- low, device address and function code 0 and IN- low places the console control word on the data bus. The Processor executes the CCW instruction and transfers data between the console and the target register or memory (as defined by bits 0 thru 15 of the CCW). Upon completion of the transfer, the Processor stops.



* PROCESSOR GENERATED SIGNAL

Figure 9-3. Register Entry/Display Sequence.

9.3.3 Step Mode Operation (Figure 9-4)

The Step Mode causes the Processor to fetch one instruction from memory, execute the instruction and then stop. The Step Mode operation can be performed only when the Processor is stopped and the console RUN switch is activated. Activiation of the RUN switch causes the START- signal to go low. Approximately 1600 nanoseconds later the Processor resumes operation on the trailing edge of START-.

The Processor, upon resumption of operation, fetches the next instruction from memory (as defined by the current value of the program counter) and executes it. The console, upon seeing the trailing edge of IF-, generates SERV-. Upon completion of the execution of the instruction fetched from memory, the Processor fetches a Stop CCW from the console, executes the instruction, and then stops.

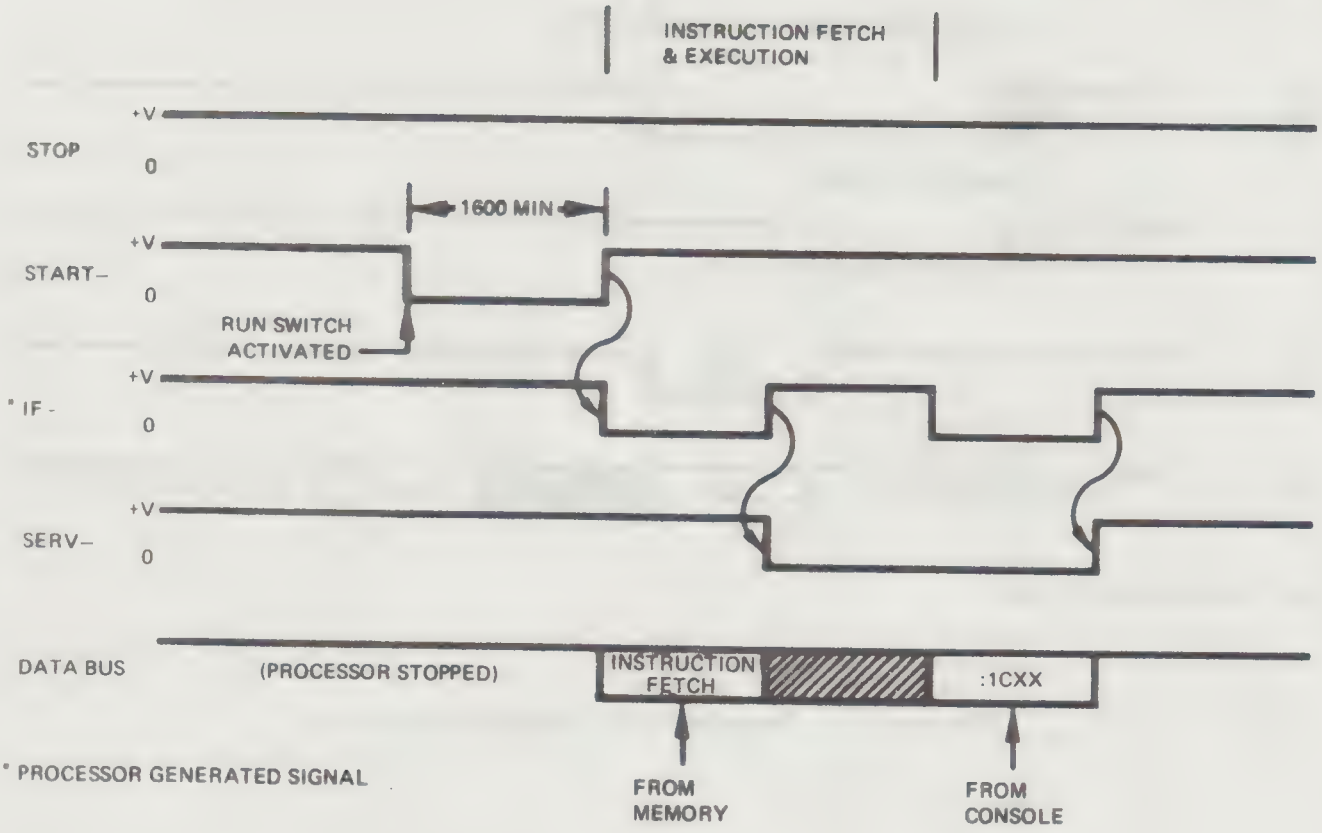
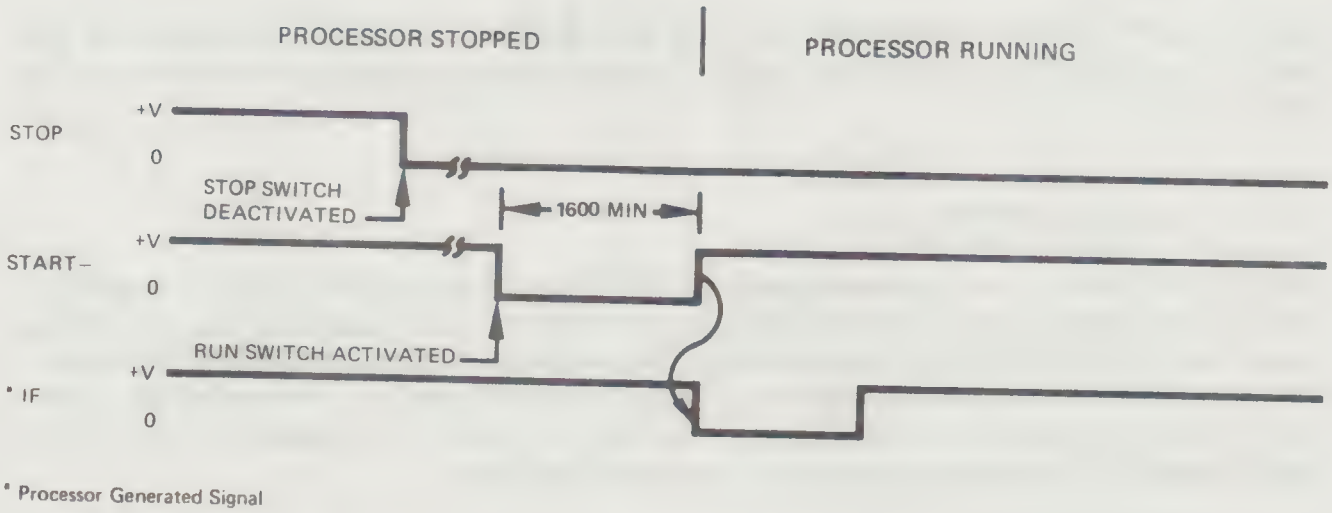


Figure 9-4. Stop Mode Sequence.

9.3.4 Establishment of Run Mode (Figure 9-5)

The Run Mode is established by deactivation of the console STOP switch and activation of the console RUN switch. Activation of the RUN switch causes the START- signal to go low. Approximately 1600 nanoseconds later, the Processor resumes operation on the trailing edge of START-.



* Processor Generated Signal

Figure 9-5. Establishment of Run Mode.

9.4 CONSOLE WORD FORMATS (Figure 9-6)

The NAKED MINI LSI uses four different word formats to convey information between the console and the Processor. These word formats are as follows:

1. Computer Status Word
2. Console Sense Word
3. Console Data Word
4. Console Control Word

9.4.1 Computer Status Word

The Computer Status Word permits the program to store volatile sense register data during a power failure and to restore the sense register data during restart operations. This capability is required with the standard ALPHA LSI console since the sense data is stored in a volatile storage register. If non-volatile toggle switches are used, this capability is not required.

The Computer Status Word is transferred between the console and the Processor, when IF- is false, using special unconditional Input or Output instructions with a device address and function code of 0. During an SIA or SIX instruction, the console copies the state of the SENSE switch (SSW) into bit 3 of the word and the contents of the Sense register (DS0 thru DS3) into bits 4 thru 7, respectively. The internal Processor status (bits 0, 1 and 2) is generated concurrently within the Processor. Upon input, the Computer Status Word is loaded into either the A or X register. Note that the console can drive only bits 3 thru 7 during an SIA or SIX instruction.

During an SOA or SOX instruction, bit 3 of the Computer Status Word contains the new state of the SENSE switch and bits 4 thru 7, respectively, contain the new state of DS0 thru DS3.

9.4.2 Console Sense Word

The Console Sense Word is transferred from the console to the Processor in response to an unconditional input command with device address 0 and function Code 1. During input operation (ISA or ISX instructions), the contents of the console sense register, DS0 thru DS3, are copied into data bits 0 thru 3 of the Maxi-Bus, respectively. All other bits of the word are transferred as zeroes. No output commands are issued by the Processor in conjunction with the Console Sense Word.

9.4.3 Console Data Word

The Console Data Word is a full unsigned (absolute) 16-bit data word that is transferred between the processor and console in response to an unconditional input or output command with device address 0 and function code 4.

During routine input operations (ICA or ICX instructions), the Console Data Word is input to the Processor A or X register. Likewise, during routine output operations (OCA or OCX instructions), the Console Data Word is transferred from the Processor to the console.

During a console service sequence, the Console Data Word can be transferred to or from the Processor A, X, I or P registers as well as memory.

9.4.4 Console Control Word

The Console Control Word (CCW) is an instruction word rather than a data word. The CCW is generated by the console during a console service sequence. The operation code of the CCW resides in the bits 6 thru 15 while bits 0 thru 5 are modifier bits.

The NAKED MINI LSI is designed to respond to eleven different CCW codes. These codes are listed below:

CCW CODE (HEX)	FUNCTION
:IC00	Stop Processor
:IC02	Read data from memory, increment P and halt
:IC03	Write data into memory, increment P and halt
:IC04	Output data from A register and halt
:IC05	Input data to A register and halt
:IC08	Output data from X register and halt
:IC09	Input data to X register and halt
:IC10	Output data from I register and halt
:IC11	Input data to I register and halt
:IC20	Output data from P register and halt
:IC21	Input data to P register and halt

It should be noted that bits 1 thru 5 are mutually exclusive, namely, only one bit may be true at a time.

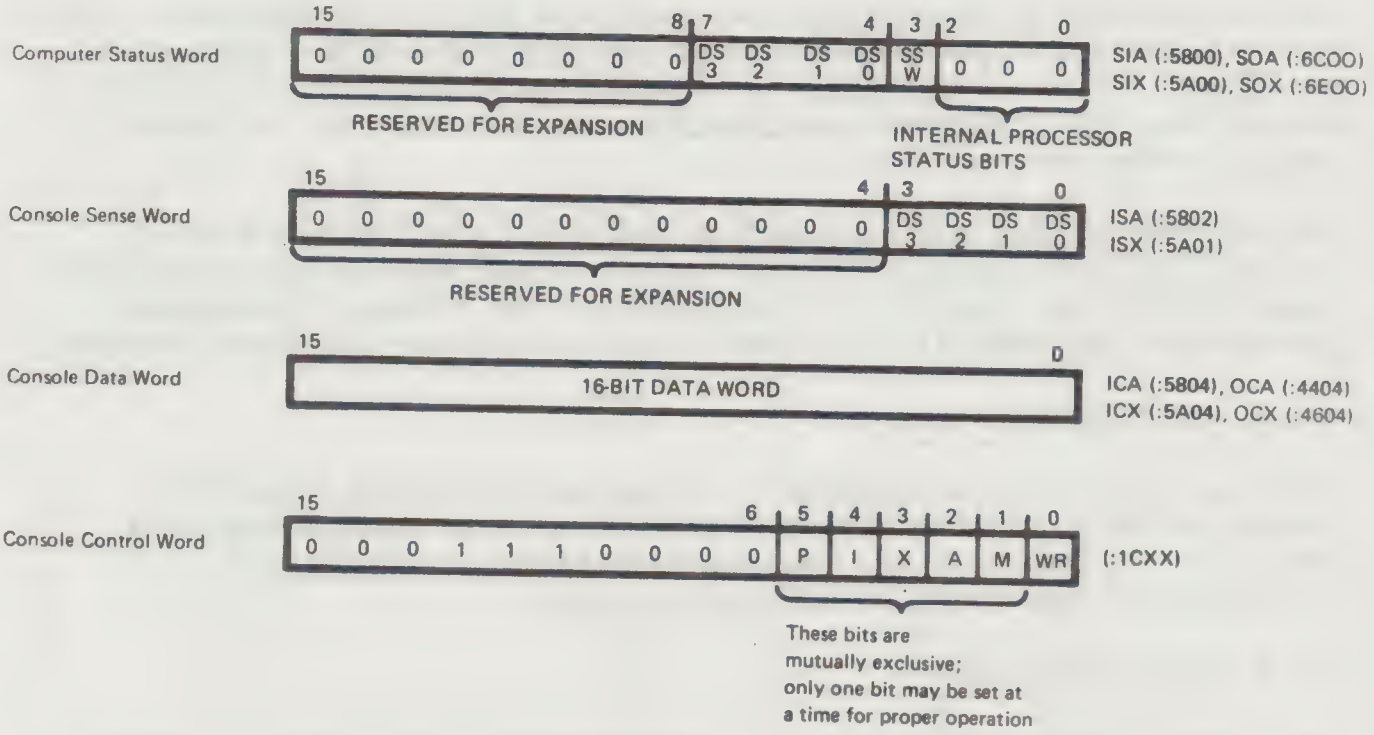


Figure 9-6. Console Word Formats

9.5 MINIMUM CONSOLE REQUIREMENTS

A minimal user designed console should have facilities to stop, reset and start the Processor as well as have system performance indicators.

9.5.1 Stopping the Processor

Stopping the Processor requires the issuance of a Console Service Request (SERV-) and the furnishing of a Stop CCW to the Processor upon recognition of SERV-.

The Processor will not recognize the Console Service Request until completion of the current instruction. Upon completion of the current instruction, the Processor recognizes the Console Service Request by initiating a CCW instruction fetch from the console rather than the normal instruction fetch from memory. The CCW transfer timing is discussed in paragraph 9.3.

The users console should be designed to furnish the CCW word during an input sequence with device address 0 and function code 0 ONLY when the instruction fetch signal (IF-) is true. Once the CCW is transferred to the Processor, the internal microprogram algorithm of the Processor brings the Processor to a stopped condition.

9.5.2 Resetting the System

Resetting the system is accomplished by forcing the System Reset signal (RST-) ground-true for a minimum of 5 microseconds. This can be accomplished with a switch or a TTL compatible open-collector signal capable of driving 32 ma. It is not necessary to synchronize or debounce this signal.

9.5.3 Starting the System

The system is started by issuance of the Start Processor signal (START-). START- is a ground-true signal that must have a minimum duration of 1.6 microseconds. START- should be driven with a 32 ma open collector TTL driver.

9.5.4 Visual Indicators

Visual indicators should be provided for ease in determining the operational status of the system. Indicators should be provided on the debounced STOP switch signal and the system RESET signal. A RUN indicator can be provided by use of a 500 microsecond retriggerable one-shot that is triggered by the memory start signal MST-. As long as the system is running, the run one-shot will be retriggered each time memory is accessed and will time-out 500 microseconds after the last memory access after departure from the Run mode. The RUN indicator should illuminate whenever the run one-shot is set.

The byte mode signal (BM-) and the overflow signal (OV-) are available for display. If these signals are applied to lamp drivers and indicators, an additional performance monitor can be obtained.

9.6 OPTIONAL CONSOLE FEATURES

The minimal console discussed in the previous paragraph can be expanded to include several additional features which are discussed in the following paragraphs.

9.6.1 Data Entry and Display

The data entry and display feature provides the capability to enter date from the console into the Processor registers or memory. Likewise, data from the Processor registers, memory or a program can be stored and displayed for operator observation.

The data entry and display feature requires that the console generate the Console Data Word. Generation of the Console Data Word requires a 16-bit register and 16 32ma open-collector drivers to drive DB00- thru DB15-. The entry switches can be applied via the storage register to the drivers. The drivers should be enabled only upon receipt of an input command with device address 0 and function code 4 (ICA or ICX).

If the user desires to accept data from the Processor, the console must have 16 data bus receivers and a 16-bit holding register. The holding register must be clocked only when a Select and Present command with device address 0 and function code 4 is received (OCA or OCX).

Diplay indicators may be tied to the outputs of the storage register and should light when a corresponding bit is true.

9.6.2 Register and Memory Display and Modification

This feature permits the operator to transfer the Console Data Word between the console and the Processor A, X, I or P register or memory.

This feature requires that, in addition to other bits, the console be able to drive DB00- thru DB05- during a Console Control Word transfer. Bits 1 through 5 of the CCW must be mutually exclusive, i.e. only one bit may be true at a time.

The console logic should be designed such that when a register select signal for bits 1 thru 5 of the CCW is generated, the SERV- and START- signals are generated simultaneously. Furthermore, the generation of any CCW word, other than the stop CCW (:1C00), must be enabled only when the Stop Mode is established. This is to avoid possible alteration of volatile data in a user's program during Run Mode.

9.6.3 Sense Register Entry and Display

The Sense register entry and display feature permits the operator to generate a Console Sense Word. The generation of a Console Sense Word requires that a 4-bit Sense Register be applied to four 32mA open collector data bus drivers (DB00- thru DB03-). The drivers should be enabled only upon receipt of an input command addressed to device address 0 and having a function code of 1.

9.6.4 SENSE Switch Feature

In addition to the four sense lines discussed above, the Processor will accept a SENSE switch signal (SSW-) that may be tested by program instructions. The SSW- signal must be ground- true when the SENSE switch is active.

9.6.5 Console Interrupt Feature

The console interrupt feature permits the operator to interrupt normal processing. The console interrupt feature generates signal CINT- which is sent to the Processor. The only timing restriction on CINT- is that it must remain active until the Processor recognizes the CINT request (recognition is obtained when the interrupt address request signal (IAR-) goes ground-true).

9.6.6 Autoload Initiation Controls

The Autoload initiation controls permit the operator to command the Autoload option to perform an autoload sequence. Autoload initiation should only be permitted when the system is in the Run Enable Mode (STOP and RUN swtiches are reset or off). Autoload initiation will take place whenever the AL- signal is forced ground-true. The signal must be ground-true for a minimum of 100 nanoseconds to guarantee a response from the Autoload option.

The user may use the AL- signal to set a flip-flop which, in turn, may drive an autoload indicator. A Select instruction with a device address and function code of 0 can be used to reset the flip-flop when loading is complete.

9.6.7 Step Mode Feature

The Step Mode feature permits the operator to manually step through a program one instruction at a time. The Step Mode is an extension of the Stop Mode wherein, if the RUN switch is activated while in the Stop Mode, the Processor will go into the run state, execute one instruction, recognize a console service request, process the request and then stop. Step Mode timing is discussed in paragraph 9.3.

9.7 USER CONSOLE INTERCONNECTION (Figure 9-7)

A user designed console can interface to the Processor in two different ways. If the user has the motherboard assembly, the console can be interfaced at connector J1. If the motherboard is not employed in the users system, the console can be interfaced directly to connector P1 of the Processor.

Motherboard connector J1 will accept a 50-pin 3M connector (Part number 3451-0000). This connector is designed to accommodate a SCOTCHFLEX™ ribbon cable (3M part number 3365-50). A printed circuit board transition adapter (3M part number 3456) is also available for the console end of the ribbon cable. Note that power and ground are available at J1 in addition to all signals required for a console. The pin assignments for connector J1 are shown on figure 9-7.

In systems that do not have a motherboard, refer to paragraph 8.3.3 of this manual.

9.8 OPTION CARD CONSOLE ACCOMMODATIONS

The NAKED MINI LSI Option Card provides console skeleton logic. Included in the logic are the following capabilities:

1. Secondary Console Sense register. Grounding four jumper pins introduces corresponding logic '1' bits in the Console Sense register word for ISA and ISX instructions. Satisfies requirements of paragraph 9.6.3.

2. Secondary Console SENSE switch. A ground jumper on the pin simulates the Console SENSE switch in a set state for SIA, SIX and conditional jump instructions. Satisfies requirements of paragraph 9.6.4.

3. Secondary Console interrupt switch. A momentary ground jumper simulates a console interrupt. This jumper option is also available at the TTY interface connector. Satisfies requirements of paragraph 9.6.5.

4. Secondary Autoload switch. A momentary ground jumper simulates the console autoload signal and results in the execution of the autoload sequence. This jumper option is also available on the TTY interface connector. (Jumper is active at all times and will first reset the computer if pressed while the computer is running.) Satisfies requirement of paragraph 9.6.6.

5. Secondary Reset switch. A momentary ground jumper simulates the console reset signal (RST-). Satisfies requirements of paragraph 9.5.2.

Each of the above capabilities and their implementation are discribed in Section 11 of this manual.

CONSOLE CONNECTOR
(3M 3415-0000)

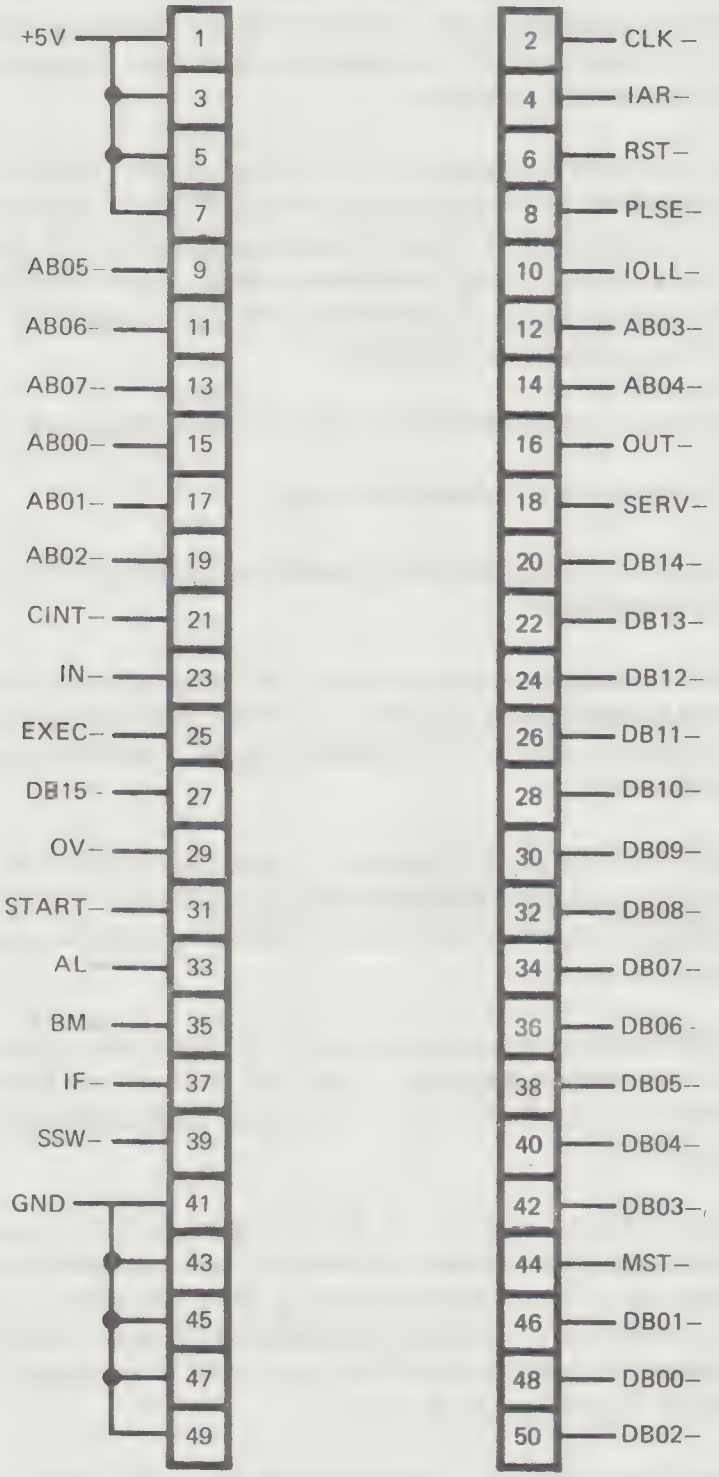


Figure 9-7. Motherboard/ Console Connector (J1) Pin Assignments

Table 9-1. Console Special Signal Load/Drive Summary

SIGNAL	CPU	CONSOLE
SSW-	5,6	2
IF-	2,6	5
AL-	5,6	2
BM-	2,6	5
OV-	2,6	5
START-	2,5,6	2
SERV-	2,5,6	2
CINT	5,6	2

Device types are as follows:

2. = 32ma open-collector driver (7438 or equivalent)
5. = TTL receiver (7400 or equivalent)
6. = Pullup resistor (1 Kohm)

Section 10

POWER SUPPLY INTERFACE REQUIREMENTS

10.1 INTRODUCTION

This section discusses the requirements of a user furnished power supply. Among the items discussed are DC power requirements, power monitor facilities, an optional AC line synchronized timing source and interconnection requirements.

10.2 DC POWER REQUIREMENTS

The user designed power supply must produce four voltages: +5 Vdc, +12 Vdc, -12 Vdc, and +5 H (hangpower). The +5 volt supply provides the VCC voltage for most integrated circuits in the Processor, Memory and I/O modules. The +12 and -12 volt supplies are used by the Processor and Memory modules and by the MOS LSI integrated circuits. Certain analog and communications options use +12 and -12 Vdc. The +5 H hangpower supply is used exclusively by the Processor; a detailed discussion of the +5 H supply is provided in paragraph 10.3. All four DC voltages share a common ground system referred to as logic ground.

10.2.1 Estimating DC Current Requirements

Before a user can design a power supply, the current requirements of each DC supply must be determined. The current load of most standard modules built by Computer Automation, Inc. are listed in table 10-1. The load currents listed are worst case for each module. The user can determine actual power requirements for his system configuration by summing the load currents for each standard module (and multiples thereof) along with the load currents of any user designed controllers.

10.2.2 Overvoltage and Reverse Voltage Protection

It is recommended that the +5 Vdc power supply employ overvoltage and reverse voltage protection devices. The overvoltage device must prevent the +5 Vdc output from exceeding +6.5 volts in the event of a power supply failure or an accidental application of a high voltage potential from an external source. Each supply output should have circuitry to prevent damage to its load or the supply itself in the event that one supply is shorted to another or to ground.

Table 10-1. Standard Module Load Currents

ASSY. NO.	COMMON NAME		DC CURRENT (AMPS) +5V	+12V	-12V
53537-XX	NAKED MINI LSI-1 With 2/4/8K Hi Drive Core Memory	- ACTIVE	5.3	6.5	5.22
		STANDBY	5.0	0.5	0.47
53538-XX	NAKED MINI LSI-1 With 1/2/4K Semiconductor Memory	- ACTIVE	3.5	1.2	0.52
		STANDBY	3.5	0.7	0.52
53506-0C	NAKED MINI LSI TYPE II		6.5		
53504-XX	2/4/8K Lo Drive Core Memory Module	- ACTIVE	3.0	0.5	2.6
		STANDBY	2.6	0.25	0.20
53526-XX	4/8/16K Hi Drive Core Memory	- ACTIVE	2.8	6.5	4.9
		STANDBY	2.5	0.5	0.15
53514-XX	1/2/4/8K MOS Memory Module	- ACTIVE	1.0	1.2	0.20
		STANDBY	1.0	0.7	0.20
53501-00	ALPHA LSI Console		1.5		
53505-XX	Option Card (maximum configuration)		1.5	0.03	0.14
53213-00	16-bit I/O Module		1.5	-----	-----
53214-XX	32-bit Relay Contact Output Module		1.5	-----	-----
53215-00	32-bit Relay Contact Input Module		1.5	-----	-----
53216-00	64-bit Output Module		1.5	-----	-----
53219-00	64-bit Input Module		1.5	-----	-----
53220-00	16 Channel Priority Interrupt Module		1.5	-----	-----
53222-00	I/O Drive Module		1.5	-----	-----
53223-00	Utility I/O Interface		1.5	-----	-----
53224-XX	Magnetic Tape Interface		3.0	-----	-----
53227-XX	103/202 Data Set Controller		1.5	0.05	0.05
53236-XX	Dual TTY/CRT Interface		1.5	0.05	0.05
53240-XX	Cassette Interface		2.5	0.190*	0.190*
53513-00	Synchronous Modem Controller		1.20	0.15	0.15
53512-XX	Asynchronous Modem Multiplexer		3.0	0.30	0.30
53530-00	Moving Head Disk Controller no. 1		3.5	-----	-----
53531-00	Moving Head Disk Controller no. 2		3.0	-----	-----

* A maximum of four cassette drives

10.2.3 Ripple and Noise Requirements

The regulator and output filter design of each power supply must be adequate to limit ripple, noise and voltage transients to 50 millivolts peak-to-peak.

10.2.4 Turnon/Turnoff Overshoot

Turnon/turnoff overshoot should not exceed two percent (2%) of the nominal voltage output of each DC power supply.

10.2.5 Regulation Requirements

Each DC power supply should maintain a regulation envelope of ±2 percent of nominal output voltage from 0 to 100 percent of full rated load over the expected range of input line voltage and over a termperature range of 0°C to 50°C.

These regulation requirements must be maintained at the Processor module. Remote sensing must be employed when voltage drops in the power supply wiring are of sufficient magnitude to cause voltage regulation to exceed ±2 percent when the load current is varied from no load to full load.

10.2.6 DC Power Storage

The +5 Vdc, +12 Vdc and -12 Vdc power supplies must have sufficient storage in the regulators to insure regulated output for at least 2 milliseconds after a power failure has been detected (refer to paragraph 10.3 for details on power fail detection).

10.3 POWER MONITOR FACILITIES (Figures 10-1 and 10-2)

The Power Monitor Facilities must develop a +5 H (hangpower) voltage and a ground-true Power Failure Detected signal (PFD-) for the exclusive use of the Processor. These provisions are required whether the Processor Power Fail/Restart option is used or not.

10.3.1 +5 H (Hangpower) Regulator

The +5 H power supply must provide auxilliary +5 Vdc power for use by the Processor to assure proper start-up and shutdown. The +5 H supply must be the first DC voltage to come into regulation upon application or restoration of AC line power and the last DC voltage to drop out of regulation upon loss or removal of AC line power.

The +5 H supply must provide 200 milliamps of DC current at +5 Vdc and regulate this voltage to within ±5 percent of nominal. Ripple and noise must be within 50 millivolts peak-to-peak. The +5 H supply must be in regulation at all times that the +5 Vdc and ±12 Vdc supplies are above 10 percent of their specified values.

10.3.2 Power Fail Detector

The power fail detector must sense when the nominal AC line voltage falls below its minimum sustaining level. When this minimum sustaining level is sensed, the power fail detector must generate a ground-true PFD- signal for use by the Processor.

The power fail detector must also have a timing function that turns off the +5, +12 and -12 Vdc regulators a minimum of 2 milliseconds after PFD- goes low.

When the AC line voltage rises above the minimum sustaining level, the power fail detector must turn on the +5, +12 and -12 Vdc regulators after allowing for a change buildup in the storage capacities of each regulator. The PFD- signal must remain in the ground-true state for a minimum of 2 milliseconds after the +5, +12 and -12 Vdc regulators have reached 98 percent of their nominal values.

The PFD- signal driver must have a minimum drive capability of 32 milliamps dc and must be collector OR- able. The driver may be implemented with either discrete elements or with an integrated circuit. The logic level for PFD- are as follows:

true = 0.0 to 0.45 Vdc
false = 2.4 to 5.0 Vdc

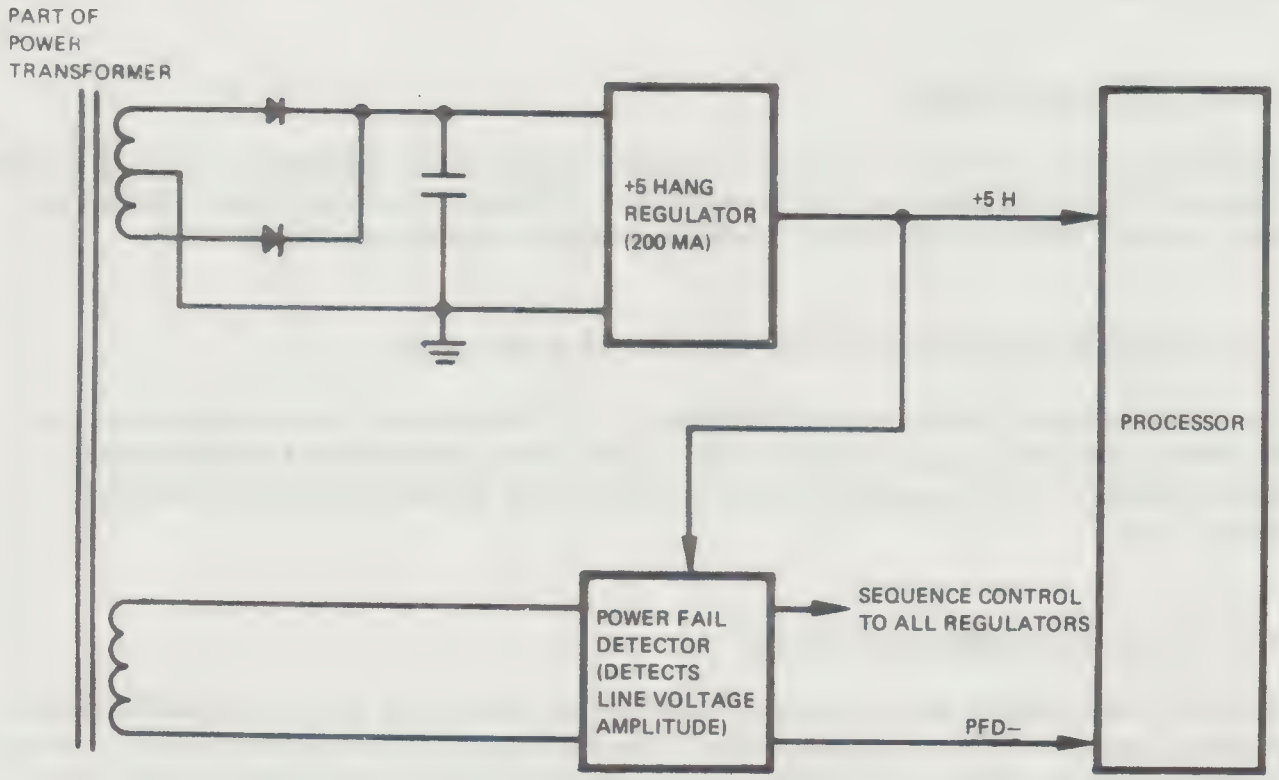
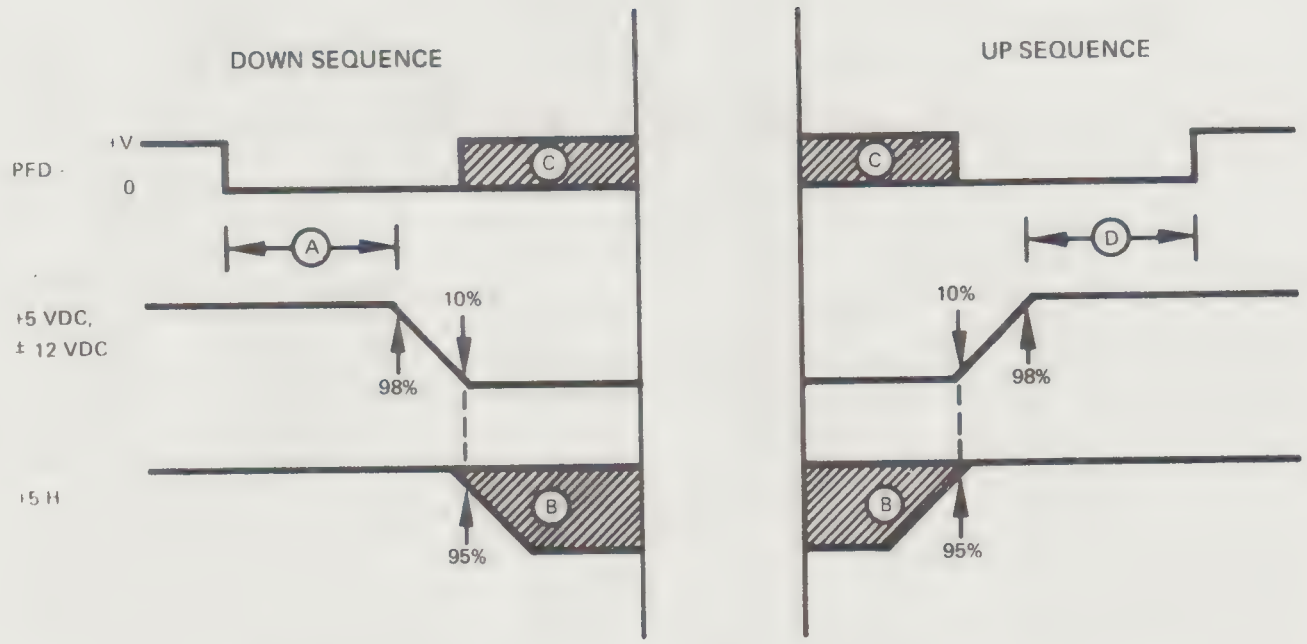


Figure 10-1. Power Monitor Block Diagram.



(A) Time = 2 milliseconds min. from falling edge of PFD– until first regulated voltage drops out
(B) +5 H voltage level undefined when +5 vdc and ±12 vdc are ≤ 10% of nominal
(C) Pfd- undefined when +5 H is ≤ 95% of nominal
(D) Time = 2 milliseconds min. from 98% point to rising edge of PFD–

Figure 10-2. Power Monitor Timing Requirements.

10.4 AC LINE SYNCHRONIZED TIMING SOURCE (OPTIONAL)

The Processor Real-Time Clock option (RTC) has provisions for a timing source input which is twice the AC line frequency. The RTC option represents only one TTL load to the timing source. The timing source output must be a TTL compatible logic signal with rise and fall times of less than 50 nanoseconds. With regard to the duty cycle of the signal, the only requirement is that the signal be ground-true a minimum of 100 nanoseconds. The Processor refers to this timing signal as TTLF- (twice the line frequency). The logic levels for TTLF- are as follows:

true = 0.0 to 0.45 Vdc
false = 2.4 to 5.0 Vdc

10.5 INTERCONNECTION REQUIREMENTS (Figures 10-3 and 10-4)

The user furnished power supply may be interfaced to the computer system in two ways, at the motherboard or directly at the Processor.

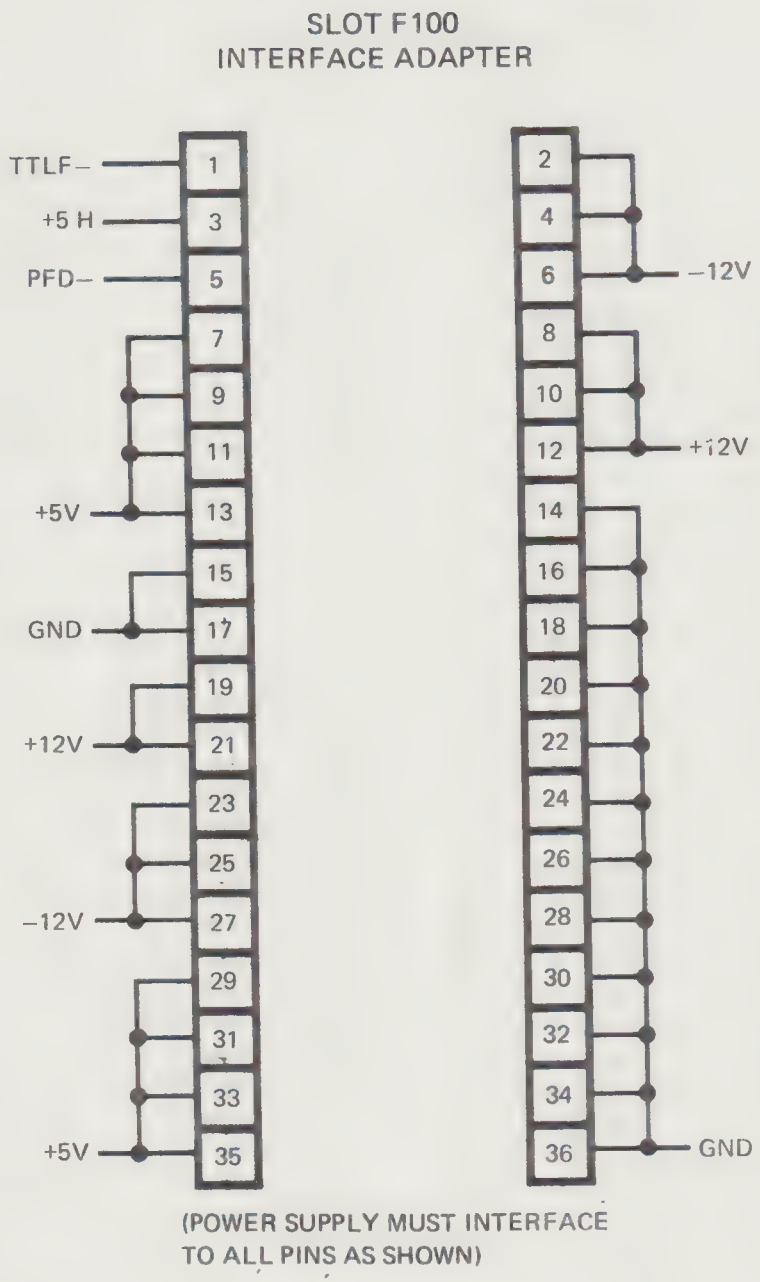


Figure 10-4. Motherboard Power Adapter Pin Assignments.

Section 11

OPTION CARD CONNECTIONS

11.1 INTRODUCTION

This section describes how to use the various features of the Teletype/CRT/Modem Controller, the Real-Time Clock (RTC), the Autoload (AL) options and the Basic Variables (BV) package which are contained on the Processor Option Card. These features are selectable by means of external jumpers on connectors located on the rear edge of the card.

The most common operating modes require no external jumpers. Unjumpered mating connectors are supplied with the Processor Option Card.

11.2 REAR EDGE CONNECTORS (Figure 11-1 and 11-2)

The rear edge of the Processor Option Card has two connectors designated J1 and J2. Connector J1 is used to select various operating modes via external jumpers while connector J2 is used to interface to a Teletype, CRT or Modem. J1 is designed to accommodate a 50-pin Viking connector (2VH25/1JN5). J2 is designed to accommodate a 36-pin Winchester connector (8BDJ18S). The pin assignments, signals and using option (in parenthesis) for connector J1 are shown in figure 11-1. Likewise, the pin assignments, signals and using options for J2 are shown in figure 11-2.

NOTE

All reserved pins listed in figures 11-1 and 11-2 are not to be used for any purpose.

Both J1 and J2 feature two rows of contacts. The contacts for J1 are designated 1 thru 50 with odd-numbered pins 1 thru 49 interfacing with the component side of the option card and even-numbered pins 2 thru 50 with the solder side of the option card. The contacts for J2 are designated A thru V and 1 thru 18. Pin A thru V interface with the component side of the option card while pins 1 thru 18 interface with the solder side of the card.

Connector J1 should be installed with connector pins 1 and 2 to the right when viewed from the rear of the computer. Connector J2 has the signals brought out in such a way that when interfacing with an ASR-33 or ASR-35 teletype, the connector may be installed right-side up or up-side down with no ill effects. When used with terminals other than a Teletype, J2 must be installed with pins A and 1 to the right as viewed from the rear of the computer.

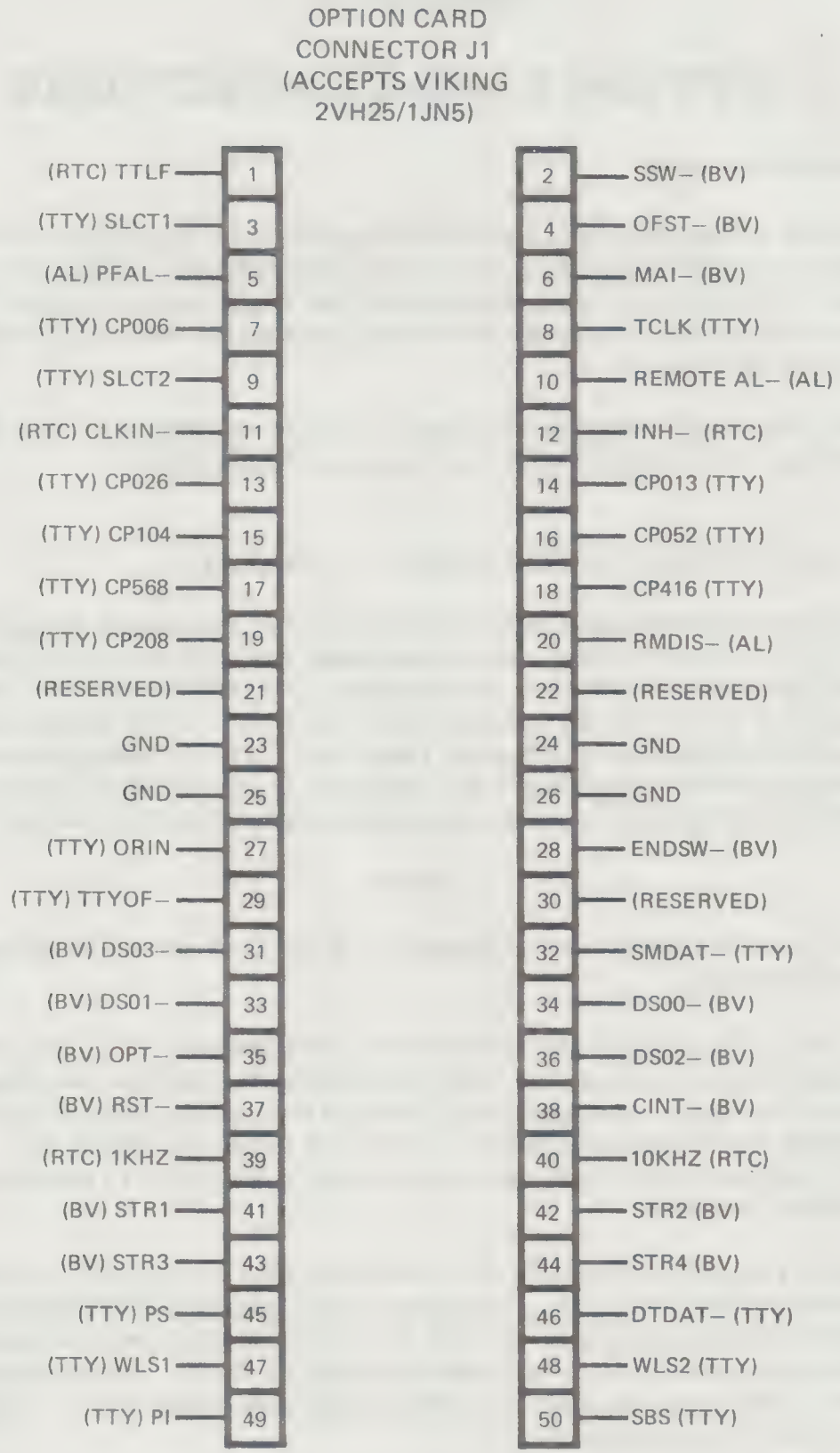


Figure 11-1. Option Card Connector J1 Pin Assignments

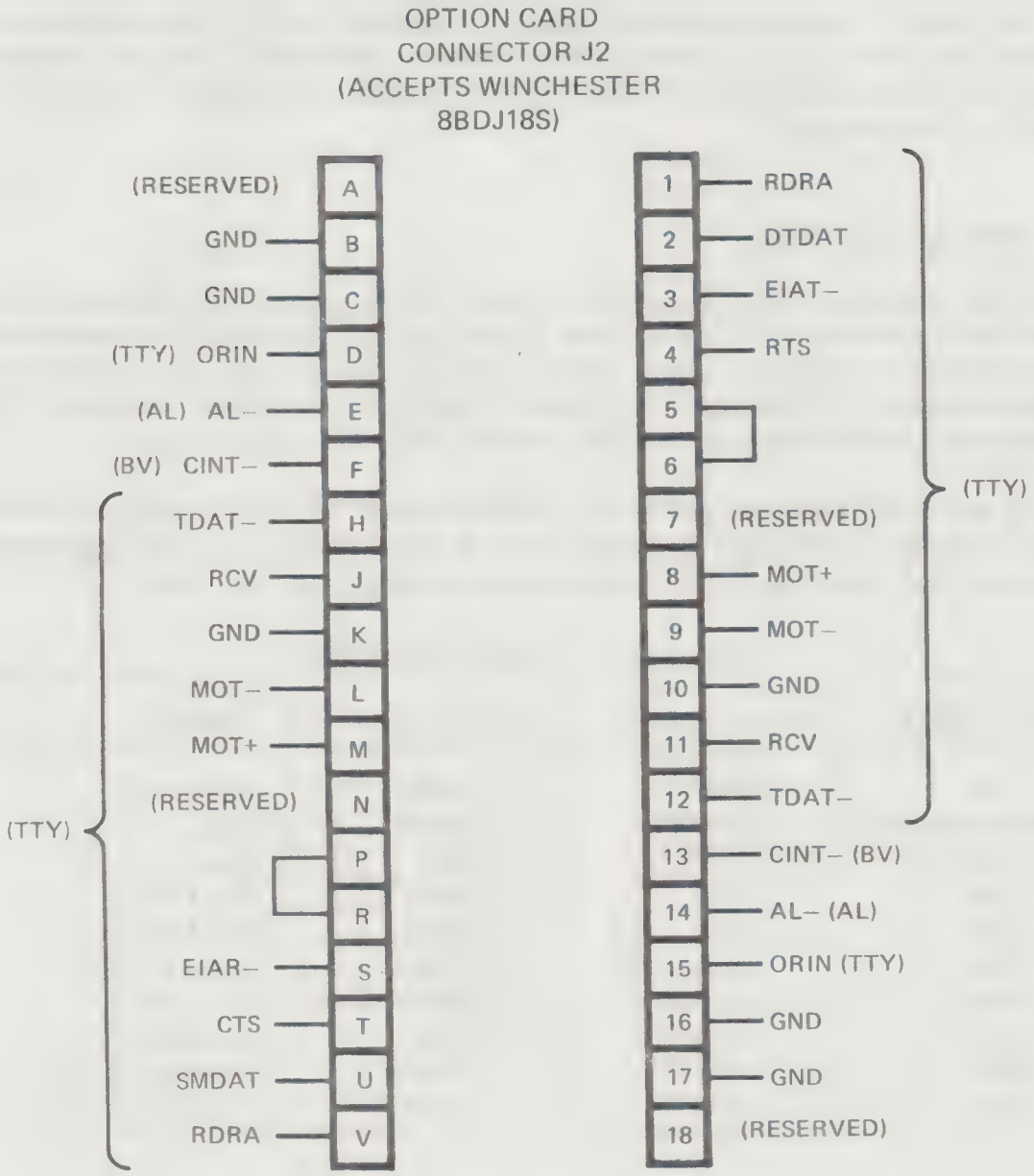


Figure 11-2. Option Card Connector J2 Pin Assignments

11.3 TELETYPE/CRT CONTROLLER

The TTY/CRT controller has provisions for ten different baud rates, a variable length word, with or without parity, and either one or two stop bits. Additionally, the user can select a current loop data path for teletypes, a TTL compatible data path, or an EIA RS232C/CCITT data path for various terminals. The user should consult the terminal manufacturers literature to determine the exact interface requirements of the terminal.

11.3.1 Baud Rate Selection

The TTY/CRT controller uses a variable format counter to provide internal clock timing for the data channel. Two counter inputs (SLCT1 and SLCT2) determine the count pattern to be employed. Eight counter outputs are brought out to connector J1. One of these outputs (CP006, CP013, CP026, CP052, CP104, CP208, CP416 or CP568) can be jumpered to the TCLK terminal to provide the right clock period.

The SLCT1 and SLCT2 signals are static control signals that are either grounded or left open. Ground is available on pins 23 thru 26 of connnector J1. The grounding configurations for selecting the various baud rates are shown in Table 11-1.

Table 11-1. Baud Rate Selection

BAUD RATE	SLCT1 (pin 3)	SLCT2 (pin 9)	JUMPER
75	GND	OPEN	Pin 8 to 17
110 (standard)	OPEN	OPEN	none
134.5	OPEN	GND	none
150	GND	OPEN	Pin 8 to 18
300	GND	OPEN	Pin 8 to 19
600	GND	OPEN	Pin 8 to 15
1200	GND	OPEN	Pin 8 to 16
2400	GND	OPEN	Pin 8 to 13
4800	GND	OPEN	Pin 8 to 14
9600	GND	OPEN	Pin 8 to 7

11.3.2 Word Length Selection

The user may select either 5-, 6-, 7- or 8-bit character lengths for the controller to process. Character length selection is controlled by WLS1 and WLS2 (pins J1-47 and J1-48,respectively). These signals are static control signals that are either grounded or left open. Ground is available on pins 23 thru 26. The grounding configurations for word length selections are shown in Table 11-2.

Table 11-2. Word Length Selections

WORD LENGTH	WLS1 (pin 47)	WLS2 (pin 48)
5-bits	GND	GND
6-bits	OPEN	GND
7-bits	GND	OPEN
8-bits (standard)	OPEN	OPEN

11.3.3 Parity Selection

The user can choose to have parity error processing, with a subsequent parity error interrupt if desired. Two signals control parity in the controller. Parity Inhibit (PI, J1-49) when open - disables parity. When PI is grounded, the parity generation and check functions are enabled and a parity bit is inserted into the transmitted word. When parity is enabled, the Parity Select signal (PS, J1-45) determines whether even or odd parity is generated by the transmit function and checked by the receive function. When PS is open, even parity is selected. When PS is grounded, odd parity is selected.

11.3.4 Stop Bit Selection

All terminal equipment requires either one or two stop bits. The Stop Bit Select signal (SBS, J1-50) provides this selection capability. When SBS is grounded, one stop bit is inserted in the transmitted word. When SBS is open, two stop bits are inserted in the transmitted word. Note, the selection of two stop bits when programming a 5-bit word generates 1.5 stop bits.

11.3.5 Alternate Interrupt Locations

When using the TTY/CRT controller in the half-duplex mode, the standard TTY/CRT interrupt locations of : 0002 and : 0006 may be changed to : 0022 and : 0026, respectively by grounding TTYOF- (J1-29). Note that this feature is automatically overridden when operating in the full-duplex mode.

11.3.6 Data Interface Selection

The user has a choice of three types of data interface that can be used with a terminal device. These interface types are current loop, RS232C/CCITT and TTL/DTL compatible.

11.3.6.1 Current Loop Interface (Figure 11-3)

The current loop interface utilizes a 3-wire ground common interface which is characterized by the presence or absence of a 20 milliamp dc signalling current. The current loop interface converts logic signals to current signals and vice-versa as follows:

mark = 20 mA current flow
space = no current flow

The controller current loop transmit signal is TDAT-, while the controller receive signal is RCV-. TDAT- is available on connector J2 at pins H and 12. RCV- enters the controller at J2 pins J and 11. A logic ground reference between the controller and the terminal device is required and is available on J2 pins K and 10.

The controller current loop receive and transmit circuits have a 1500 ohm, 1 watt resistor in series with their respective lines. These resistors are used to set the current level on each line to 20 mA dc. The current loop receive line also has a built-in roll-off filter which limits baud rates to 150 baud maximum.

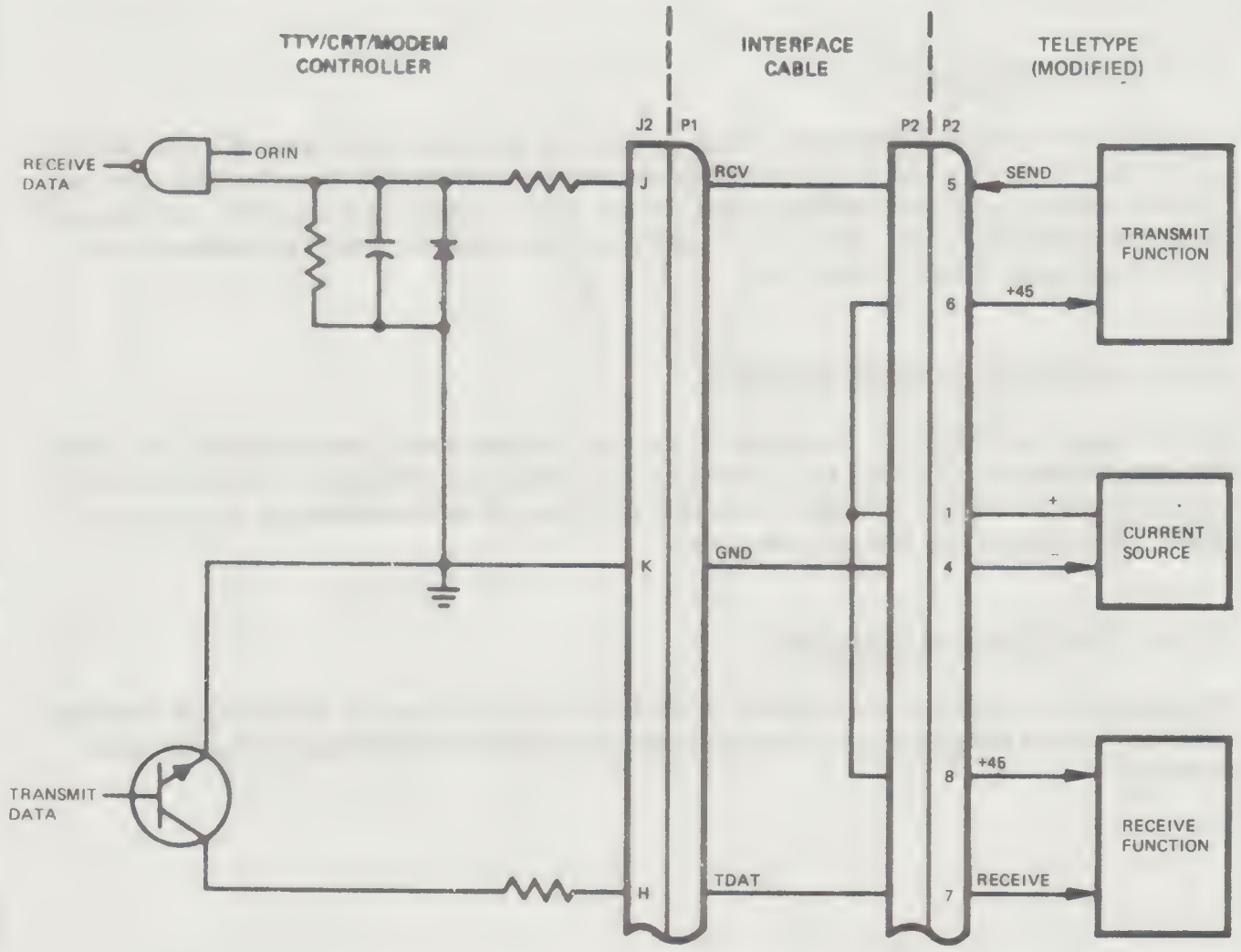


Figure 11-3. Current Loop Interface

11.3.6.2 EIA RS232C/CCITT Interface (Figure 11-4)

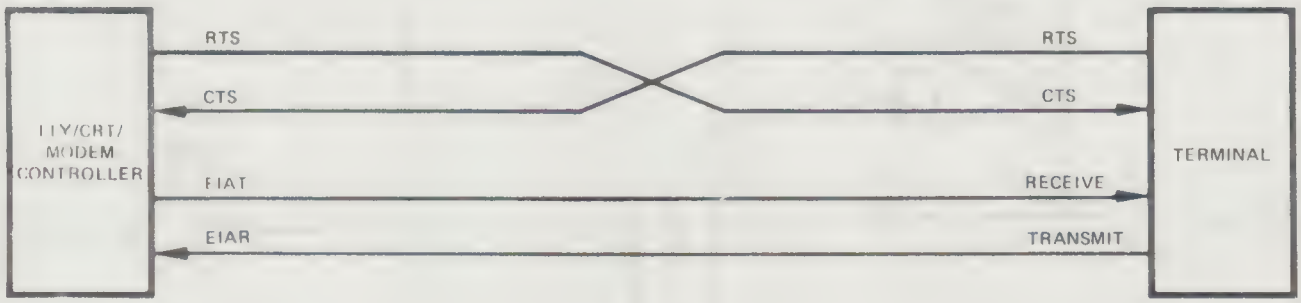
The EIA RS232C/CCITT interface (EIA) uses signal levels which vary between plus and minus seven volts. The interface provides two control signals in addition to receive transmit data signals. The interface signal levels are as follows:

data:	mark = -7 Vdc
	space = +7 Vdc
control:	true = +7 Vdc
	false = -7 Vdc

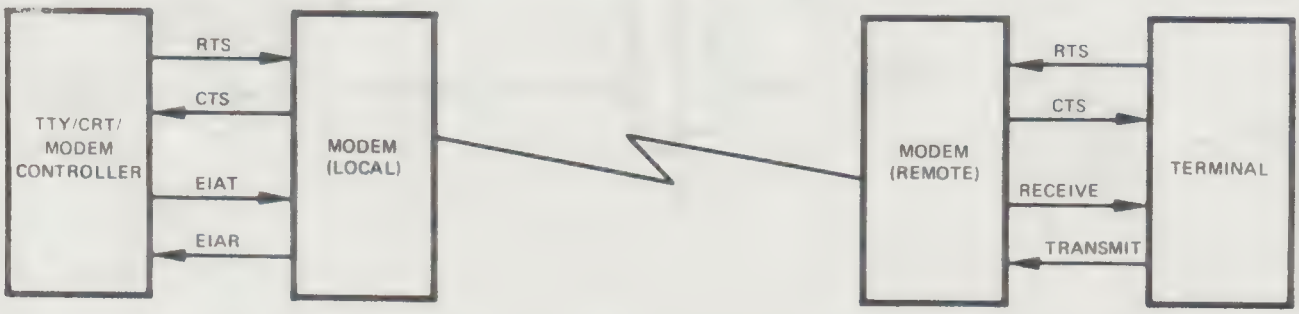
The controller EIA receive signal is designated EIAR- and is available on J2 pin S. The EIA transmit signal is designated EIAT- and is available on J2 pin 3. The two EIA control signals are Request-to-Send (RTS) and Clear-to-Send (CTS). RTS is available at J2 pin 4 while CTS enters the interface at J2 pin T.

The RTS and CTS lines from both the controller and the terminal device are defined for operation with a modem. When operating without a modem (direct interface as shown in figure 11-4a), the RTS and CTS lines must be crossed.

With the RTS and CTS control lines crossed, half-duplex switching from receive mode to transmit mode and vice-versa is controlled by the controller RTS line. When the controller RTS line is true, the terminal device transmits to the controller. When the controller RTS line is false, the controller transmits to the terminal device. During full-duplex operation, the RTS line of both the controller and the terminal device must be true for simultaneous transmission.



a. Interface without Modem.



b. Interface with Modem.

Figure 11-4. EIA RS 232C/CCITT Interface

When operating with a half-duplex modem, carrier keying by means of the RTS signal is not used to switch from transmit to receive modes. Instead, End-of-Message (EOM) character detection within the support software is used. When operating with a full-duplex modem, no special disciplines are required.

The Request-to-Send signal (RTS) is generated by the controller motor on/off flip-flop. The motor on/off flip-flop has delay circuitry which disables the controller sense multiplexer for 600 milliseconds after receipt of a motor on command. When using the motor on/off flip-flop with an EIA device, the delay circuitry must be disabled. The delay circuits are disabled by grounding the ORIN- input, J1 pin 27 or J2 pins D and 15.

11.3.6.3 TTL/DTL Compatible Interface (Figure 11-5)

The TTL/DTL compatible interface (TTL) uses signal levels which vary from 0 to +5 volts dc. The interface signal levels are as follows:

mark = 0.0 to 0.45 Vdc
space = 2.4 to 5.0 Vdc

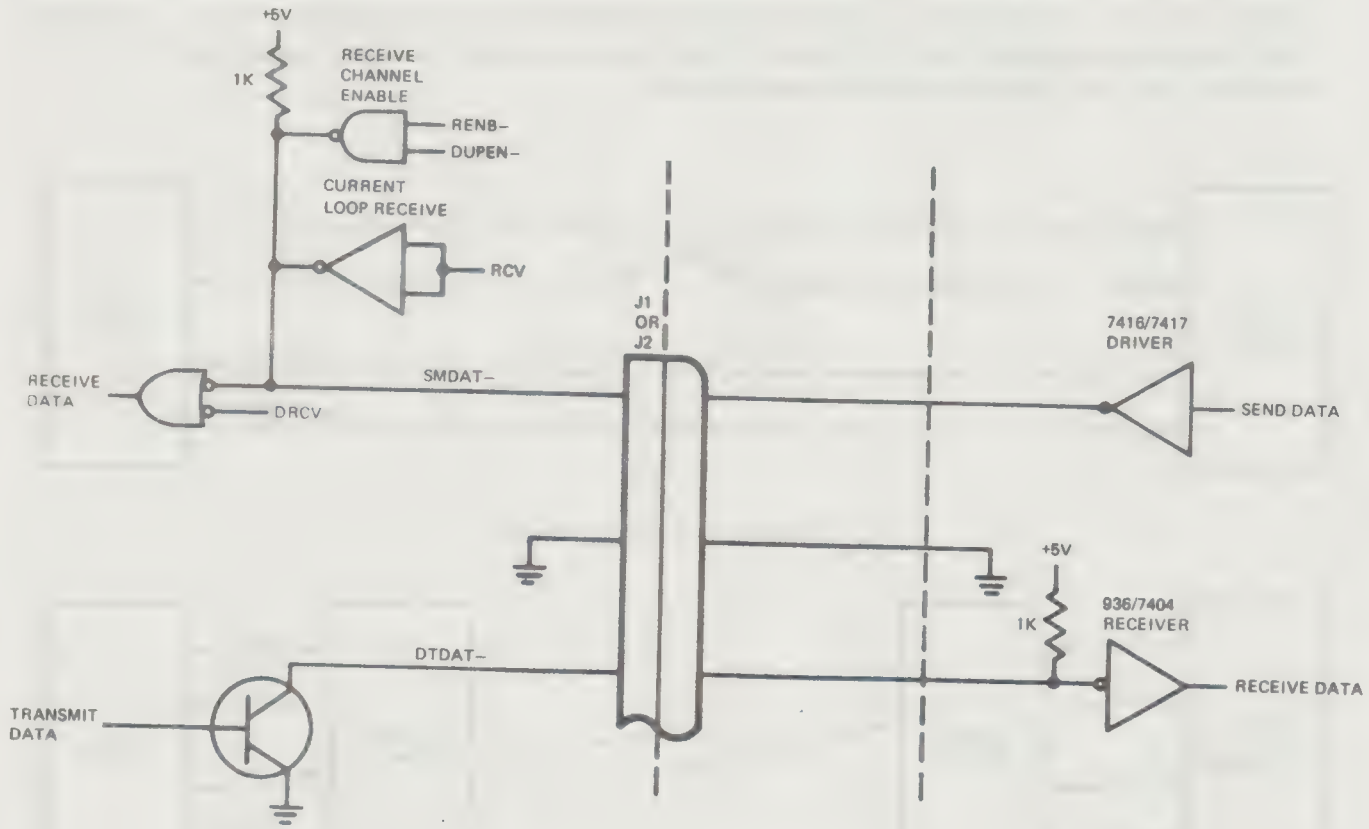


Figure 11-5. TTL/DTL Interface

The TTL receive signal is SMDAT- which is available at J1 pin 32 and J2 pin U. SMDAT- should be driven by an open-collector driver in the terminal device. The controller represents only one load to the driver. The controller provides a 1K ohm pull-up resistor to +5 Vdc. The TTL transmit signal is DTDAT- and is available on J1 pin 46 and J2 pin 2. DTDAT- is driven by the controller with an open-collector driver which is capable of 50 milliamps dc drive current. The terminal device must provide a pull-up resistor to the terminal VCC supply which must now exceed 100 volts dc.

11.3.7 Special Teletype Controls

The Teletype/CRT controller contains provisions which permit user generated software to control paper tape reader and drive motor turn/on and turn/off in specially modified ASR-33 and ASR-35 Teletype units.

The reader control signal is designated RDRA and is available at J2 pins V and 1. The motor control signals are referred to as MOT+ and MOT- and are available at J2 pins M and 8, and L and 9, respectively.

11.4 REAL-TIME CLOCK

With no jumper installed, the Real-Time Clock (RTC) option operates off a built-in 100 Hz timing source. The user can select four other timing sources (10 kHz, 1kHz, twice the AC line frequency (TTLF) or a TTL compatible external timing source).

The RTC option represents only one TTL load to the external timing source. The external timing source must be a TTL compatible logic signal with rise and fall times of less than 50 nanoseconds. With regard to duty cycle, the only requirement is that the signal be ground-true with a minimum of 100 nanoseconds.

When the user desires to select an alternate timing source (other than the standard 100 Hz source), the 100 Hz clock source must be inhibited by grounding the INH- input. Clock source selection can be accomplished at connector J1 using Table 11-3.

Table 11-3. Clock Source Selection

CLOCK SOURCE	INH- (pin 12)	JUMPER CONNECTIONS
100 Hz (standard)	OPEN	none
1,000 Hz	GND	Pin 39 to pin 11
10,000 Hz	GND	Pin 40 to pin 11
TTLF	GND	Pin 1 to pin 11
EXTERNAL*	GND	User Timing source to pin 11

*External timing source must be TTL/DTL compatible.

11.5 AUTOLOAD

Two optional features are available for controlling the Autoload option. Remote Autoload initiation and automatic Autoload upon restoration of power.

11.5.1 Remote Autoload Inititation

The functions of the console AUTO switch can be duplicated by momentarily grounding (i.e. a switch closure to ground) pin 10 on connector J1 or pins E or 14 on connector J2. The signal must be ground-true for a minimum of 100 nanoseconds to be recognized by the Autoload option.

11.5.2 Automatic Autoload

An Autoload sequence can be automatically initiated upon restoration of power by jumpering J1 pin 20 (RMDIS-) to J1 pin 5 (PFAL-). This feature is particularly useful when using volatile memories without battery backup power. With this feature, memory is automatically reloaded with an operational program from a peripheral storage device after power is restored.

11.6 BASIC VARIABLES PACKAGE

The Basic Variable Package permits the user to operate high priority (Processor) interrupts independent of EIN/DIN control, offset interrupts, extend I/O transfer timing and perform certain console functions in the absence of a console.

11.6.1 Independent Processor Interrupt Operation

In normal operation, the power fail, console and TRAP interrupt (referred to as Processor-generated interrupts) will not be recognized by the Processor if interrupts are not enabled (DIN instruction has disabled recognition of ALL interrupts). The EIN instruction must be executed before any interrupts can be processed.

By grounding the OPT- signal (J1 pin 35), the Processor generated interrupts can obtain immediate recognition by the Processor when they are enabled.

With J1-35 grounded, the PFE and PFD instructions control the Power-Fail/Restart interrupt while the CIE and CID instructions control console interrupts. There are no control instructions for a trap interrupt other than the TRP instruction itself.

11.6.2 Interrupt Offset

All interrupts (except power-up) generated within the Processor and the Processor Option Card may be relocated (offset) from the scratchpad area of memory by : 100 locations to allow for more efficient utilization of the scratchpad area.

Two types of offset are available on connector J1. The high priority Processor interrupts (power fail,console interrupt,and TRAP) and the high priority user generated interrupts (IL1 and IL2) can be offset by grounding the OFST- signal (J1 pin 4). Likewise, the low priority Teletype/CRT controller and Real Time Clock option interrupts can be offset by grounding the MAI- signal (J1 pin 6).

11.6.3 Secondary Console Sense Register

The Basic Variables Package contains four jumpers which permits the user to simulate the console sense register and develop a Console Sense Word in the absense of a console. The jumper inputs are DS00- (J1 pin 34), DS01- (J1 pin 33), DS02- (J1 pin 36) and DS03 (J1 pin 31). DS00- is the least significant bit of the simulated register, while DS03- is the most significant bit. Grounding a particular jumper input introduces a logic "1" into the corresponding bit position of the Console Sense Word. A logic "0" is introduced when a given input is left open.

The entire simulated register is enabled by grounding the ENDSW- signal which is available at J1 pin 28. Note that all control logic required to respond to the ISA (:5801) and ISX (:5A01) instructions is also provided with this feature. This feature cannot be used when a console is installed.

11.6.4 Secondary Console Switch Functions

Secondary console SENSE, RESET and INT switch signals which duplicate the functions of the console are available to the user. The SSW- signal (J1 pin 2) duplicates the SENSE switch, RST- (J1 pin 37) duplicates the RESET switch and CINT- (J1 pin 38 and J2 pins F and 13) duplicates the INT switch.

These switch functions are generated by taking the input pin to ground (momentarily). RST must be ground-true a minimum of 5 microseconds. SSW- must remain at ground when the SENSE switch is active.

11.6.5 I/O Timing Extension

The Basic Variables Package features an I/O stretch capability which permits the user to slow down the I/O transfer timing when driving the Maxi-Bus through multiple expansion chassis or over long distances. Four strap connections (STR1, STR2, STR3 and STR4) permit the user to specify 16 different increments of stretch.

The NAKED MINI LSI Type 1 uses stretch increments of 200 nanoseconds, while the Type 2 Processor has stretch increments of 100 nanoseconds. Based on these increments, the Type 1 Processor stretch can range from 0 to 3000 nanoseconds while the Type 2 Processor stretch can range from 0 to 1500 nanoseconds.

Note that whenever any stretch is inserted, all I/O timing throughout the system is slowed down. This can have an adverse effect on speed critical I/O devices and in general reduces Processor throughput.

The stretch strapping scheme for both the Type 1 and Type 2 Processor is shown in Table 11-4. Ground is available on pins 23 thru 26 of connector J1.

Table 11-4. I/O Stretch Selection

STRETCH ADDITION (Nsec)		STRAP CONFIGURATION			
TYPE 1 PROCESSOR	TYPE 2 PROCESSOR	STR4 (J1-44)	STR3 (J1-43)	STR2 (J1-42)	STR1 (J1-41)
0	0	OPEN	OPEN	OPEN	OPEN
200	100	OPEN	OPEN	OPEN	GND
400	200	OPEN	OPEN	GND	OPEN
600	300	OPEN	OPEN	GND	GND
800	400	OPEN	GND	OPEN	OPEN
1000	500	OPEN	GND	OPEN	GND
1200	600	OPEN	GND	GND	OPEN
1400	700	OPEN	GND	GND	GND
1600	800	GND	OPEN	OPEN	OPEN
1800	900	GND	OPEN	OPEN	GND
2000	1000	GND	OPEN	GND	OPEN
2200	1100	GND	OPEN	GND	GND
2400	1200	GND	GND	OPEN	OPEN
2600	1300	GND	GND	OPEN	GND
2800	1400	GND	GND	GND	OPEN
3000	1500	GND	GND	GND	GND

Appendix A

RECOMMENDED DEVICE AND INTERRUPT ADDRESSES

A.1 GENERAL

Table A-1 and A-2 list recommended Device and Interrupt Addresses to prevent possible conflict during future expansion to other I/O modules.

Table A-1. Recommended Device Addresses

DEVICE	DEVICE ADDRESSES	
	STANDARD	ACTUAL
Refer to Table A-3*	00	
	01	
Dual TTY/CRT (TTY1/CRT1)	02	
Dual TTY/CRT (TTY0/CRT0)	03	
Line Printer (LP)	04	
Card Reader (CR)	05	
Paper Tape Punch (PTP)	06(17)	
Paper Tape Reader (PTR)	06	
Processor TTY* (TTY)	07	
Real Time Clock* (RTC)	08	
Magnetic Tape (Mag Tape)	09	
	0A	
	0B	
	0C	
Synchronous Modem Controller (SCM)	0D	
Asynchronous Modem Multiplexer (AMM)	0E	
Disc	0F	
Cassette	10	
	11	
16-Bit I/O (A/D System)	12	
	13	
Plotter	14	
	15	
32-Bit Relay In (RCIM)	16	
Punch Alternate	17	
16-Bit Input/Output (16-Bit I/O)	18	
64-Bit Input (64-Bit In)	19	
64-Bit Output (64-Bit Out)	1A	
Priority Interrupt Module (PIM)	1B	
32-Bit Relay Out (RCOM)	1C	
103 Data Set Controller (103 DSC)	1D	
	1E	
	1F	

* not alterable

( ) Indicates suggested alternate.

Table A-2. Scratchpad/Page 0, Recommended Interrupt Address Map

	00-1F	20-3F	40-5F	60-7F	80-9F	A0-BF	C0-DF	E0-FF
0	:00* POWER UP	:20* 64-BIT OUT			:80 PIM(0)		:C0 AMM RCV1	
1								
2	:02 TTY WORD	:22 MAG TAPE WORD	:42 LP WORD	:62 TTY0/CRT0 WORD	:82 PIM(1)	:A2 PLOTTER WORD		
3								
4					:84 PIM(2)		:C4 AMM XMIT1	
5								
6	:06 TTY EOB	:26 MAG TAPE EOB	:46 LP EOB	:66 TTY0/CRT0 EOB	:86 PIM (3)	:A6 PLOTTER EOB		
7								
8					:88 PIM(4)		:C8 AMM RCV2	
9								
A	:0A M.H. DISC	:2A PTR/PTP WORD	:4A CR WORD	:6A TTY1/CRT1 WORD	:8A PIM(5)	:AA RCIM WORD		
B								
C					:8C PIM(6)		:CC AMM XMIT2	
D								
E		:2E PTR/PTP EOB	:4E CR EOB	:6E TTY1/CRT1 EOB	:8E PIM(7)	:AE RCIM EOB		
F								
0	:10* 64-BIT IN	:30** 103 DSC ANSWER	:50 CASSETTE ADDRESS		:90 PIM(8)		:D0 AMM RCV3	
1								
2	:12 MEMORY PARITY	:32** 103 DSC INPUT WORD	:52 CASSETTE WORD	:72 16-BIT I/O WORD	:92 PIM(9)	:B2 AMM EXCEPTION		
3								
4					:94 PIM(10)	:B4 AMM RECEIVE EOB	:D4 AMM XMIT3	
5								
6		:36** 103 DSC IN EOB	:56 CASSETTE EOP	:76 16-BIT I/O EOB	:96 PIM(11)	:B6 AMM XMIT EOB		
7								
8	:18 RTC CLOCK	:38** 103 DSC PAR ERR/FLT			:98 PIM(12)		:D8 AMM RCV4	
9								
A	:1A RTC SYNC	:3A** 103 DSC OUTPUT WORD	:5A RCOM WORD	:7A 16-BIT I/O WORD	:9A PIM(13)			
B								
C	:1C POWER DOWN				:9C PIM(14)		:DC AMM XMIT4	
D								
E	:1E CONS INT & TRAP	:3E** 103 DSC OUT EOB	:5E RCOM EOB	:7E 16-BIT I/O EOB	:9E PIM(15)			
F								

XX = Interface Generated Interrupt Address
* = Non-Alterable Address
** = Locations 30-3F are reserved for Autoload option, if used (103 DSC addresses must be relocated.)

EOB = End-of-Block
EOP = End-of-Operation

Table A-3. Device Address 0 Command Summary

FUNCTION CODE	SELECT COMMANDS	SENSE COMMANDS	INPUT COMMANDS	OUTPUT COMMANDS
0	Terminate Autoload Sequence	Autoload Option Installed	SIA (:5800), SIX (:5A00)	SOA (:6C00), SOX (:6E00)
1	Initiate Autoload Sequence	Real-Time Clock Option Installed	ISA (:5801) ISX (:5A01)	SIN 0 (:6801)
2	PFE (:4002)			SIN 1 (:6802)
3	PFD (:4003)			SIN 2 (:6803)
4	OCA (:4404) OCX (:4604)	TTY/CRT/Modem Option Installed	ICA (:5804) ICX (:5A04)	SIN 3 (:6804)
5	CIE (:4005)			SIN 4 (:6805)
6	CID (:4006)			SIN 5 (:6806)
7	TRP (:4007)			SIN 6 (:6807)

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